8 kW high power density and high frequency PSU for AI data centers and servers

REF_8KW_HFHD_PSU

About this document

Scope and purpose

This document introduces a new, complete power supply unit (PSU) for AI data centers and servers.

REF_8KW_HFHD_PSU can deliver 8 kW steady state maximum output power in the specified 180 V – 277 V AC input AC voltage range, with a peak efficiency of 97.5% and a minimum efficiency of 96.5% from 30% to 100% of output power at 230 V_{AC} input voltage, including fan power consumption.

With a size of just 40 mm x 73.5 mm x 450 mm (including chassis) and 100 W/in^3 power density, REF_8KW_HFHD_PSU shows a viable approach for achieving higher power density and efficiency simultaneously, in the AC/DC power conversion stage compared to current state-of-the-art solutions.

For easy implementation, REF_8KW_HFHD_PSU uses a traditional two-stage power conversion approach. The front-end interleaved totem-pole AC/DC converter provides power factor correction (PFC) and regulates the intermediate bulk, and the back-end isolated DC/DC LLC converter provides isolated and regulated 50 V_{DC} nominal output voltage from the high-voltage rail.

Furthermore, the critical hold-up time requirement is addressed by the REF_8KW_HFHD_PSU power supply in the proposed form factor, with no need of additional external circuits. The PSU is capable of 20 ms maximum hold-up time at 100% output load by means of an auxiliary boost converter (namely hold-up time extension circuit, or baby-boost).

Intended audience

The document is intended for R&D engineers, hardware designers, and developers of power electronic systems.

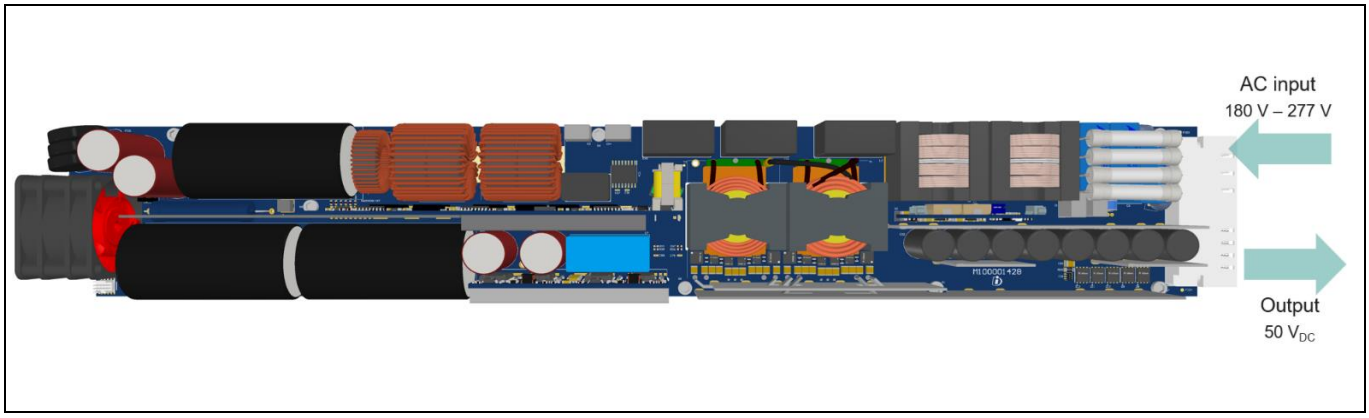


Figure 1 Overview of the REF_8KW_HFHD_PSU power supply unit

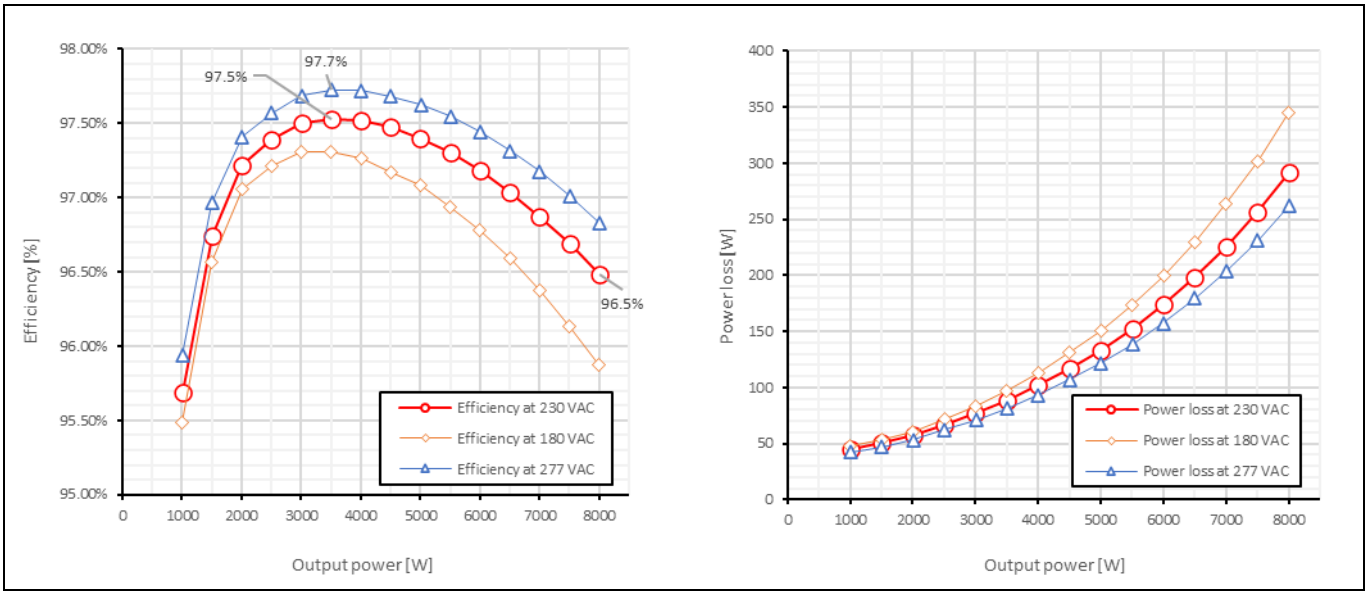


Figure 2 REF_8KW_HFHD_PSU measured efficiency including fan power consumption

The key components from Infineon enabling REF_8KW_HFHD_PSU are:

- CoolSiC™ 650 V Gen 2, 40 mΩ TOLL (IMT65R040M2H), and EiceDRIVER™ 2EDB9259Y for the fast switching boosting legs of the totem-pole PFC converter
- CoolSiC™ 650 V Gen 2, 10 mΩ TOLL (IMT65R010M2H), and EiceDRIVER™ 2EDB9259Y for the synchronous rectification leg of the totem-pole PFC converter
- 600 V CoolMOS™ CM8, 16 mΩ TOLL (IPT60R016CM8), EiceDRIVER™ 1EDN8511B, and 1EDB8275F for the static switch, the re-rush switches of the baby boost converter, and the in-rush switch
- CoolGaN™ 650 V HEMT GIT, 35 mΩ TOLL (IGT65R035D2), EiceDRIVER™ 2EDB8259Y for HB switches at the primary side of the LLC converter
- OptiMOS™ 8, 80 V, 3.3 mΩ center gate source-down (IQE033N08LM6CG), and EiceDRIVER™ 2EDB7259K for the synchronous rectification (SR) switches of the secondary side of the LLC converter
- 600 V CoolMOS™ G7, 50 mΩ (IPT60R050G7), CoolSiC™ 600 V diode (IDL12G65C5), and EiceDRIVER™ 1EDB8275F for the baby boost converter
- ISOFACE™ 4DIR1400H digital isolator for the primary to secondary isolation in the LLC converter
- XMC4200-Q48K256 microcontroller for the implementation of the PFC control

Table of contents

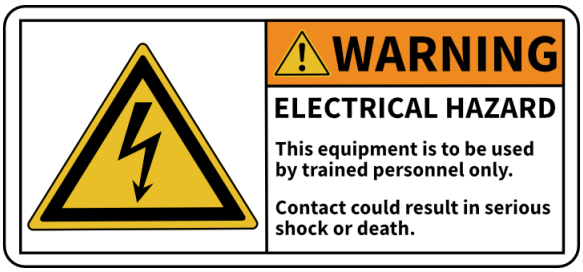
About this document **1**
Table of contents **3**
Safety information **5**
Important notice **5**
Safety precautions **6**
1 Background and specifications **7**
1.1 Application background 7
1.2 The OCP ORv3 specification 7
1.3 Key features of the 8 kW PSU 7
1.4 Electrical performance of the 8 kW PSU 9
2 System overview and description **12**
2.1 System overview 12
2.2 Topology selection 12
2.3 Power stage control and protections 14
2.4 Highlighted products 14
2.5 Hardware implementation 16
2.5.1 PFC and LLC power daughter cards 17
2.5.2 LLC transformer implementation overview 18
2.6 PSU efficiency and losses 19
3 Topology blocks description **20**
3.1 Bridgeless interleaved totem-pole PFC 20
3.1.1 Performance of the topology block standalone 20
3.1.2 EMI filter magnetics 22
3.1.3 PFC magnetics 24
3.1.4 Control scheme of the PFC 25
3.1.5 Sensing in the PFC converter 26
3.1.6 Driving CoolSiC™ and CoolMOS™ switches 27
3.2 High frequency LLC resonant converter 30
3.2.1 Performance of the standalone topology block 30
3.2.2 LLC integrated transformer and inductors 32
3.2.3 Driving CoolGaN™ and OptiMOS™ switches 35
3.3 Hold-up time extension, in-rush, and re-rush current control 37
4 Experimental results **40**
4.1 Steady-state performance 40
4.1.1 PSU efficiency and power losses 40
4.1.2 PSU power factor correction and iTHD 40
4.1.3 PSU startup 41
4.1.4 Output and bulk voltage ripple 43
4.1.5 Bridgeless interleaved totem-pole PFC 45
4.1.6 Full-bridge to full-bridge LLC converter 46
4.1.7 Thermal performance 47
4.2 Dynamic performance 49
4.2.1 Output load transients 49
4.2.2 AC input voltage sag 50
4.2.3 Hold-up time extension and re-rush current limit circuits 51

Table of contents

4.3 EMI measurements 52
5 Summary 56
6 List of figures 57
7 Bill of materials 59
8 Schematics 65
References 71
Acronyms/abbreviations 72
Revision history 73
Disclaimer 74

Safety information

Please read this document carefully before starting up the device.





Important notice

Evaluation boards, demonstration boards, reference boards and kits are electronic devices typically provided as an open-frame and unenclosed printed circuit board (PCB) assembly. Each board is functionally qualified by electrical engineers and strictly intended for use in development laboratory environments. Any other use and/or application is strictly prohibited. Our boards and kits are solely for qualified and professional users who have training, expertise, and knowledge of electrical safety risks in the development and application of high-voltage electrical circuits. Please note that evaluation boards, demonstration boards, reference boards and kits are provided “as is” (i.e., without warranty of any kind). Infineon is not responsible for any damage resulting from the use of its evaluation boards, demonstration boards, reference boards or kits. To make our boards as versatile as possible, and to give you (the user) opportunity for the greatest degree of customization, the virtual design data may contain different component values than those specified in the bill of materials (BOM). In this specific case, the BOM data has been used for production. Before operating the board (i.e. applying a power source), please read the application note/user guide carefully and follow the safety instructions. Please check the board for any physical damage, which may have occurred during transport. If you find damaged components or defects on the board, do not connect it to a power source. Contact your supplier for further support. If no damage or defects are found, start the board up as described in the user guide or test report. If you observe unusual operating behavior during the evaluation process, immediately shut off the power supply to the board and consult your supplier for support.

Operating instructions

Do not touch the device during operation, keep a safe distance. Do not touch the device after disconnecting the power supply, as several components may still store electric charge and can discharge through physical contact. Several parts, like heatsinks and transformers, may still be very hot. Allow the components to discharge and cool before touching or servicing. All work such as construction, verification, commissioning, operation, measurements, adaptations, and other work on the device (applicable national accident prevention rules must be observed) must be done by trained personnel. The electrical installation must be completed in accordance with the appropriate safety requirements.

Safety precautions

Note: *Please note the following warnings regarding the hazards associated with development systems.*

Table 1 Safety precautions

	**Warning:** *The evaluation or reference board contains DC bus capacitors, which take time to discharge after removal of the main supply. Before working on the converter system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *The evaluation or reference board is connected to the AC input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the converter before you disconnect or reconnect wires or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heatsink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the converter, power electronics and associated equipment should plan, install, commission, and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A converter that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as under sizing the cabling, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*

1 Background and specifications

1.1 Application background

The growing demand for power in AI applications has created a pressing need for power conversion solutions that are both highly efficient and compact. To support the development of next-generation data center infrastructure, power supplies must deliver high efficiency and high power-density. This requires the whole power conversion chains such as the AC/DC, the intermediate bus converter (IBC), and the voltage regulator module (VRM) stages to be capable to provide high power to the data processing hardware (e.g. GPUs, etc.) in a small form factor compared to past requirements.

The REF_8KW_HFHD_PSU reference design from Infineon demonstrates a viable approach for achieving higher power density and efficiency simultaneously in the AC/DC power conversion stage compared to current state-of-the-art solutions.

1.2 The OCP ORv3 specification

The Open Compute Project v3 5.5 kW specification [1] has been considered as the guideline for the efficiency profile and the dimensions of the unit during the design stage. To ensure a high power-density solution that is viable, the output power has been increased to 8 kW but in a lower volume, which has been tightened from 40 mm x 73.5 mm x 640 mm of the 5.5 kW PSU as per OCP's specifications (48 W/in^3) to a suitable dimension to double the power density to 100 W/in^3, being 40 mm x 73.5 mm x 450 mm.

Additionally, among all the requirements listed in [1], the 20 ms hold-up time requirement at 100% of output load is the most impactful from a power density point of view, and a fair comparison of the power density parameter among different PSUs requires the hold-up requirement to be satisfied for all of them. Indeed, to satisfy the hold-up time requirement without a hold-up time extension circuit, a much larger capacitance would be needed, reducing the power density. The hold-up time extension circuit is therefore implemented in REF_8KW_HFHD_PSU as a viable solution to implement the 20 ms hold up time with a 100 W/in^3 power density.

1.3 Key features of the 8 kW PSU

REF_8KW_HFHD_PSU has the following features:

- 8 kW maximum output power
- 97.5% peak efficiency at 230 V_{AC}
- 96.5% efficiency at 230 V_{AC} and 100% of output load
- 40 mm x 73.5 mm x 450 mm for 8 kW including chassis (vs 40 mm x 73.5 mm x 640 mm for 5.5 kW [1])
- 100 W/in^3 power density
- 20 ms hold-up time extension at 100% of output load
- In-rush current limiting circuit with no electromechanical relays
- Re-rush current control after a line cycle dropout (LCDO) event
- Overcurrent protections on LLC primary and output currents (latching)
- AC input voltage brownout protection
- UVP and OVP protections on output voltage (latching)
- UVP and OVP protections on bulk voltage

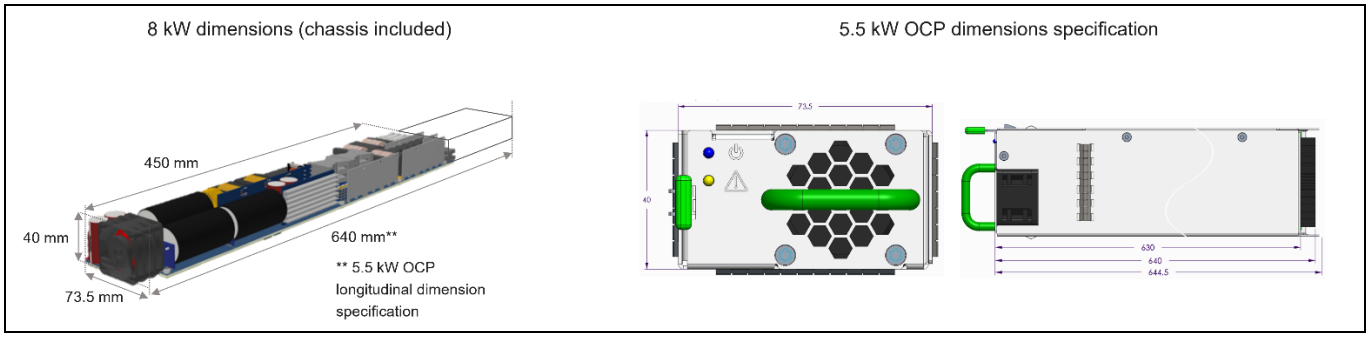


Figure 3 **Dimensions of the 8 kW power supply REF_8KW_HFHD_PSU compared to OCP v3 requirement for the 5.5 kW PSU**

1.4 Electrical performance of the 8 kW PSU

Table 1 Steady state performance of the 8 kW PSU

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
AC input supply voltage	$V_{AC,in}$	180	230	277	V	RMS value
Supply voltage frequency	$f_{AC,in}$	–	50	–	Hz	–
Nominal output voltage	V_{out}	–	50	–	V	DC, full input voltage range
Output power	–	–	–	8000	W	Full input voltage range
Operating ambient temperature	T_{amb}	–	25	–	°C	Unit verified at 25°C ambient temperature
Peak-to-peak output voltage steady-state ripple	$V_{out,rpp}$	–	–	0.2	V	100 MHz probe BW 0.1 µF capacitor locally connected
Power density	–	–	100	–	W/in^3	–
Power factor	$PF_{10\text{-}20\%}$	0.95	–	–	–	$V_{AC,in}$ = 230 V [1] 10-20% of full load
	$PF_{20\text{-}100\%}$	0.98	–	–		$V_{AC,in}$ = 230 V [2] 20-100% of full load
	$PF_{40\text{-}100\%}$	–	>0.995	–		$V_{AC,in}$ = 230 V 40-100% of full load
Input current THD	$iTHD_{5\text{-}10\%}$	–	–	12	%	$V_{AC,in}$ = 230 V [2] 5-10% of full load
	$iTHD_{10\text{-}30\%}$	–	4	7		$V_{AC,in}$ = 230 V [3] 10-30% of full load
	$iTHD_{30\text{-}100\%}$	–	3.5	4		$V_{AC,in}$ = 230 V [3] 30-100% of full load
LLC operating frequency	$f_{SW,LLC}$	380	–	540	kHz	–

[1] Minimum PF as per OCP v3 specification
$PF_{min,10\text{-}20\%}$ = 0.95; $PF_{min,20\text{-}100\%}$ = 0.98

[2] Maximum iTHD as per OCP v3 specification
$iTHD_{5\text{-}10\%}$= 15%; $iTHD_{10\text{-}30\%}$ = 10%; $iTHD_{30\text{-}100\%}$ = 5%

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
PFC operating frequency	$f_{SW,PFC}$	–	65	–	kHz	High-frequency bridge
Nominal bulk voltage	V_{bulk}	–	405	–	V	–
Peak-to-peak bulk voltage ripple	$V_{bulk,rpp}$	–	25	–	V	100% of full load

Table 2 Efficiency performance of the 8 kW PSU

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Efficiency (PSU inside chassis, cooling fan power consumption included)	$\eta_{min,230V}$	96.5	–	–	–	$V_{AC,in}$ = 230 V [3] 30-100% of full load
	$\eta_{pk,230V}$	–	97.5	–	–	$V_{AC,in}$ = 230 V [1] 30-100% of full load
	$\eta_{min,180V}$	95.8	–	–	–	$V_{AC,in}$ = 180 V [1] 10-30% of full load
	$\eta_{pk,180V}$	–	97.3	–	–	$V_{AC,in}$ = 180 V [1] 30-100% of full load
	$\eta_{min,277V}$	97.8	–	–	–	$V_{AC,in}$ = 277 V [1] 10-30% of full load
	$\eta_{pk,277V}$	–	97.7	–	–	$V_{AC,in}$ = 277 V [1] 30-100% of full load

Table 3 Protection limits in 8 kW PSU

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
AC input current limit	$I_{AC,in}$	–	–	70	A	Peak current limit on each phase
Output current OCP	$I_{OUT,OCP}$	–	165	–	A	Triggers PSU shutdown latching protection[4]
Output voltage OVP	$V_{out,OVP}$	–	58	–	V	Triggers PSU shutdown latching protection[4]

[3] Minimum efficiency values as per OCP v3 specification:
$\eta_{min,230V}$ = 96.5%; $\eta_{pk,230V}$ = 97.5%; $\eta_{min,208V}$ = 96.5%; $\eta_{pk,208V}$ = 97.5%

[4] Protection thresholds adjustable via firmware

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Output voltage UVP	$V_{out,UVP}$	–	42	–	V	Triggers PSU shutdown latching protection[4]
LLC primary current OCP	$I_{LLC-pri,OCP}$	–	34	–	A	Triggers PSU shutdown latching protection[4]
Input AC voltage brownout protection	$V_{AC,BOPon}$	–	180	–	–	PSU turn on
	$V_{AC,BOPon}$	–	176	–	V	PSU turn off

Table 4 Dynamic performance of the 8 kW PSU

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Output voltage under/overshoot during load transients	$\Delta V_{out,10-50\%}$	–	–	0.5	V	1 A/µs output load[5] change rate 10-50% of full load 50-10% of full load
	$\Delta V_{out,10-90\%}$	–	–	0.6	V	1 A/µs output load[5] change rate 10-90% of full load 90-10% of full load
Output voltage settling time during load transients	$t_{Vout,set}$	–	–	1	ms	1 A/µs output load[6] change rate 10-90% of full load 90-10% of full load
AC voltage sag transient	$V_{AC,min,50ms}$	160	–	–	V	Maximum time duration of the voltage sag: 500 ms
Hold-up time	$t_{HU,100\%}$	–	20	–	ms	100% of full load
	$t_{HU,50\%}$	–	24	–	ms	100% of full load No t_{HU} max limitation

[5] Max undershoot or overshoot according to [1]:
10-50% load step: 0.5 V 10-90% load step: 1.0 V

[6] Max settling time according to [1]: 3.0 ms

2 System overview and description

2.1 System overview

The REF_8KW_HFHD_PSU reference design is shown in Figure 4 with its chassis. The overall dimensions including the steel chassis are 40 mm x 73.5 mm x 450 mm. The backplane connector complies with ORv3 5.5 kW standards and provides both AC input and 50 V/RTN isolated DC output connections.

To achieve the power density target, a tri-dimensional mechanical assembly has been necessary and multiple daughter boards are assembled on the main PCB as shown in Figure 4. Further details about the hardware implementation are reported in Section 2.5.

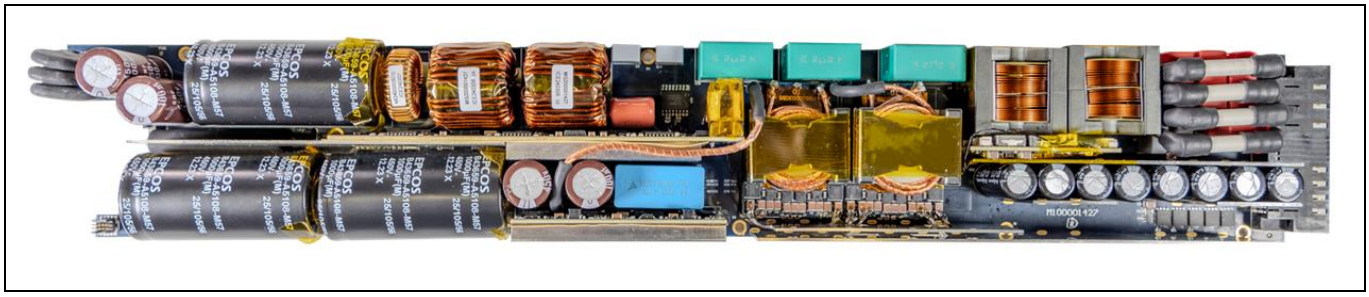


Figure 4 Top-side picture of the REF_8KW_HFHD_PSU without chassis

2.2 Topology selection

Figure 5 reports a simplified schematic of REF_8KW_HFHD_PSU.

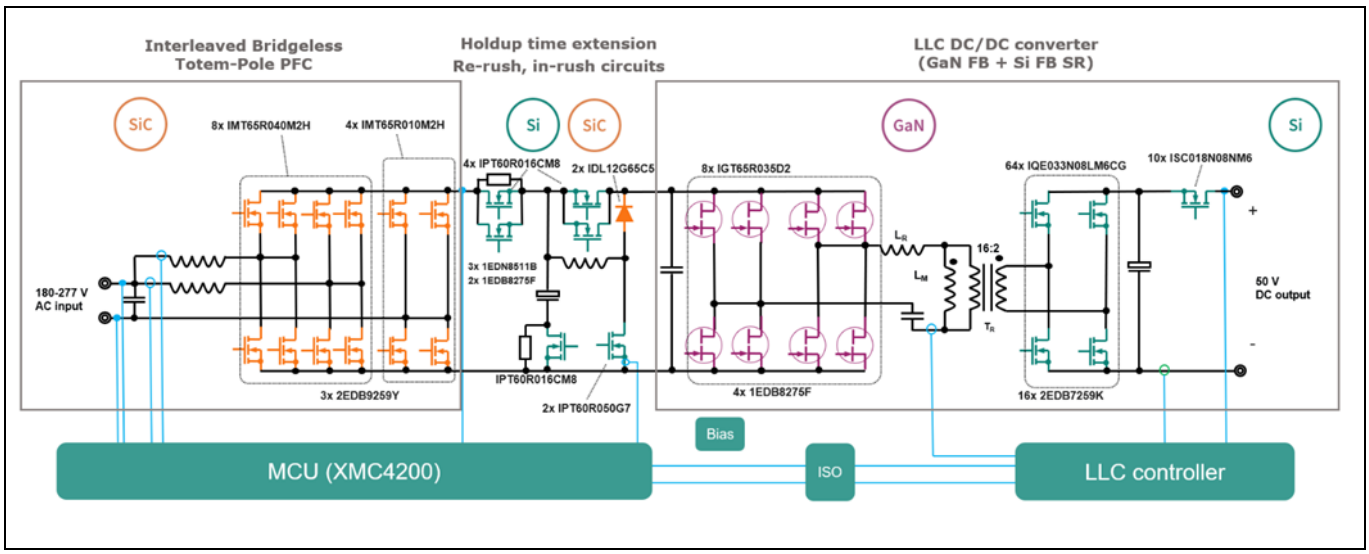


Figure 5 Simplified schematic of REF_8KW_HFHD_PSU (EMI filters not shown)

To ease the implementation, a traditional, well-known, two-stage power conversion approach has been chosen for REF_8KW_HFHD_PSU, as the feasibility study showed a possibility to meet the required efficiency.

During normal operation in steady stage, the first AC/DC conversion stage rectifies the 180 V_{AC} – 277 V_{AC} input voltage to 405 V_{DC} nominal bulk voltage, and the DC/DC conversion stage regulates the output voltage to 50 V_{DC} nominal output of the PSU.

- The first AC/DC conversion stage is a two-stage interleaved totem-pole PFC converter. Besides rectifying the AC input to 405 V_{DC}, this stage also provides power factor correction (PFC), and current total harmonic distortion (iTHD) regulation
- The second DC/DC conversion stage is a full-bridge primary, full-bridge secondary resonant LLC DC/DC converter. It provides galvanic reinforced isolation, regulates the output voltage to 50 V_{DC} nominal, and rejects the $2 \cdot f_L$ (where f_L is the AC line frequency) ripple component present on the bulk voltage.
  The overall primary-to-secondary turn ratio is 16:2 and is achieved with two similar 8:2 XFMRs (transformers) in series with integrated parallel and series resonant inductors (see Section 3.2)
- The auxiliary power circuit for in-rush/re-rush and hold-up time extension is also connected between the first AC/DC PFC and the second DC/DC conversion stage. This power block is bypassed during steady state operation and operates only during dynamic transients. It includes an in-rush circuit to limit the PSU maximum input current during startup without the need for an electromechanical relay, and a hold-up time extension circuit (namely baby-boost) that allows deep discharge of the bulk up to 20 ms hold-up time. A re-rush circuit is also provided to limit the maximum PSU input current charging the bulk capacitance after a line cycle dropout (LCDO) event

2.3 Power stage control and protections

The control of the power stages is realized with two different controller ICs, as shown in Figure 5.

The control of the AC/DC bridgeless interleaved totem-pole converter is implemented with the Infineon XMC™ 4200 microcontroller, referenced to the primary side ground. With this configuration the following are possible: power factor correction, iTHD control, output voltage regulation, and current control for each PFC boost inductor, and re-rush, in-rush, and baby boost control. From a protection point of view, XMC™ 4200 implements AC input and boost inductor currents limitation, bulk overvoltage protection (non-latching, i.e., PSU is not turned off when triggered), undervoltage lockout (UVLO), and brownout protection (latching, i.e., PSU turns off when triggered), soft-start, adaptive dead-times, and serial communication interface towards the LLC secondary-side controller.

The control of the DC/DC LLC converter is implemented with a third-party microcontroller, referenced to the secondary side ground. Because of this, the PWM of the primary side high-voltage switches are passed through an ISOFACE™ 4DIR1400H isolator for reinforced digital isolation. With this implementation of the DC/DC stage control, the following protections are achieved: output voltage regulation, load dependent adaptive dead-times, overcurrent protection on the primary resonant current (latching), output overcurrent protection (latching), output overvoltage protection (latching), output undervoltage protection (latching), soft-startup sequence, and UART communication with XMC™ 4200. The PWM for the cooling fan is also controlled by the LLC microcontroller and implements fan-stop protection (latching).

2.4 Highlighted products

Infineon power semiconductors and ICs are key in enabling 8 kW output power in the 100 W/in^3 form factor.

For the interleaved AC/DC bridgeless totem-pole PFC, a full SiC solution with paralleled MOSFETs has been used:

- Fast switching boost legs
  - 8x CoolSiC™ 650 V Gen 2, 40 mΩ TOLL (IMT65R040M2H), 2x paralleled devices per commutation slot
  - 2x dual channel EiceDRIVER™ 2EDB9259Y, one per each stage leg
- Low frequency unfolding leg
  - 4x CoolSiC™ 650 V Gen 2, 10 mΩ TOLL (IMT65R010M2H), 2x paralleled devices per commutation slot
  - 1x dual channel EiceDRIVER™ 2EDB9259Y

For the LLC DC/DC isolated converter, a hybrid solution of 650 V GaN and 80 V Si MOSFETs has been adopted for better performance and cost optimization:

- Primary side
  - 8x CoolGaN™ 650 V HEMT GIT, 35 mΩ TOLL (IGT65R035D2), 2x paralleled devices per switch
  - 4x single channel isolated drivers EiceDRIVER™ 1EDB8275F
- Secondary side synchronous rectifiers
  - 64x OptiMOS™ 8, 80 V, 3.3 mΩ center gate source-down (IQE033N08LM6CG), 8x total in each secondary-side board for both SR bridges
  - 32x dual channel isolated EiceDRIVER™ 2EDB9259Y, 2x in each secondary-side board

For the hold-up, in-rush and re-rush control circuit between the PFC and the LLC stages:

- Hold-up time extension circuit
  - 2x CoolMOS™ 600 V G7, 50 mΩ (IPT60R050G7), 2x in parallel for the active boost switch
  - 2x CoolSiC™ 650 V diodes (IDL12G65C5), 2x in parallel for the boost freewheeling diode
  - 1 x single channel non-isolated driver EiceDRIVER™ 1EDN8511B
- In-rush control circuit
  - 1x CoolMOS™ 600 V CM8, 16 mΩ TOLL (IPT60R016CM8) for the in-rush NTC bypass switch
  - 1 x single channel non-isolated driver EiceDRIVER™ 1EDN8511B
- Re-rush control circuit
  - 2x CoolMOS™ 600 V CM8, 16 mΩ TOLL (IPT60R016CM8), for the baby boost bypass switch
  - 2x CoolMOS™ 600 V CM8, 16 mΩ TOLL (IPT60R016CM8), for the re-rush resistor bypass switch
  - 2x single channel isolated driver EiceDRIVER™ 1EDB8275F

Additionally, in the PSU, the following ICs are used:

- ISOFACE™ 4DIR1400H digital isolator for the primary-to-secondary isolation in the LLC converter
- XMC4200-Q48K256 microcontroller for the implementation of the PFC control

2.5 Hardware implementation

The complete hardware implementation of the unit is shown in Figure 6 and Figure 7.

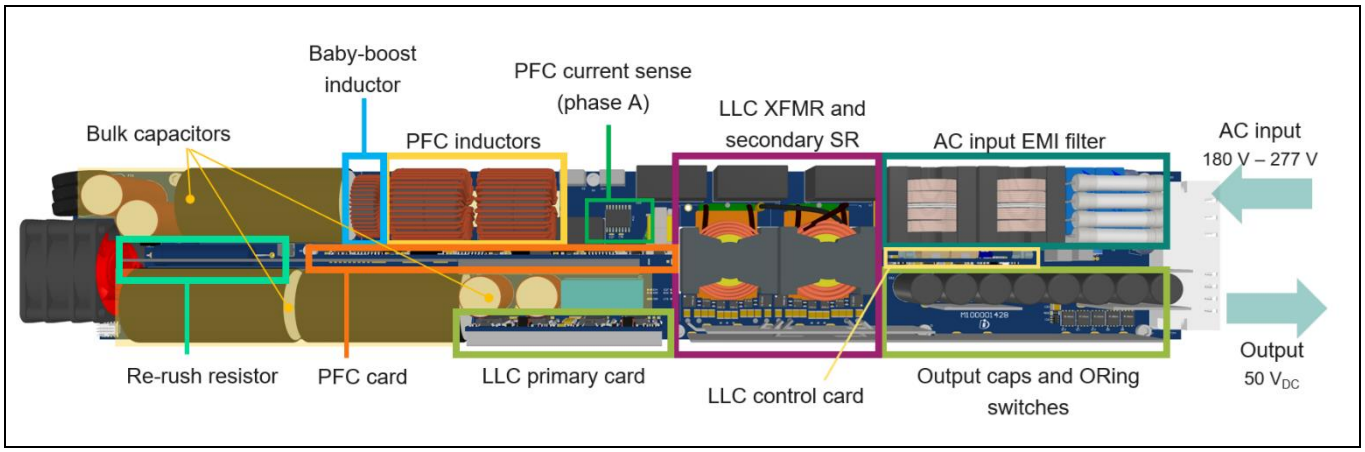


Figure 6 Hardware implementation of REF_8KW_HFHD_PSU (top side)

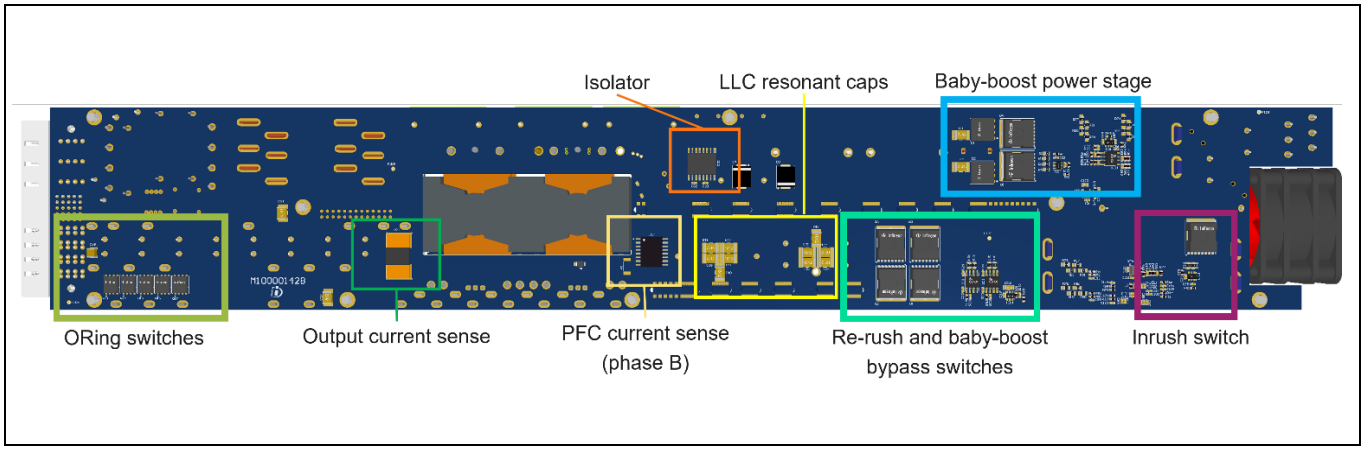


Figure 7 Hardware implementation of REF_8KW_HFHD_PSU (bottom side)

Overall, the 8 kW Infineon power supply is comprised of the following boards:

- The main board (M100001428) acting as a support for the whole PSU; it hosts the power daughter cards and the following components:
  - AC input EMI filter
  - PFC inductors, bulk capacitor bank, boost inductors current sensing, and PFC microcontroller
  - Two integrated LLC XFMRs and the primary/secondary isolator
  - Hold-up time extension circuit
  - In-rush and the re-rush circuits
  - DC output capacitors and ORing circuit
- The PFC daughter card (PW200001428)
- The LLC daughter card (PW100001427)
- The LLC control card (CD100001427)

2.5.1 PFC and LLC power daughter cards

Figure 8 and Figure 9 show respectively the PFC and LLC daughter cards as discussed in Section 2.5.

The LLC daughter card (PW100001427) hosts the primary full-bridge of the LLC DC/DC converter, together with the two isolated supplies for the two high-side switches.

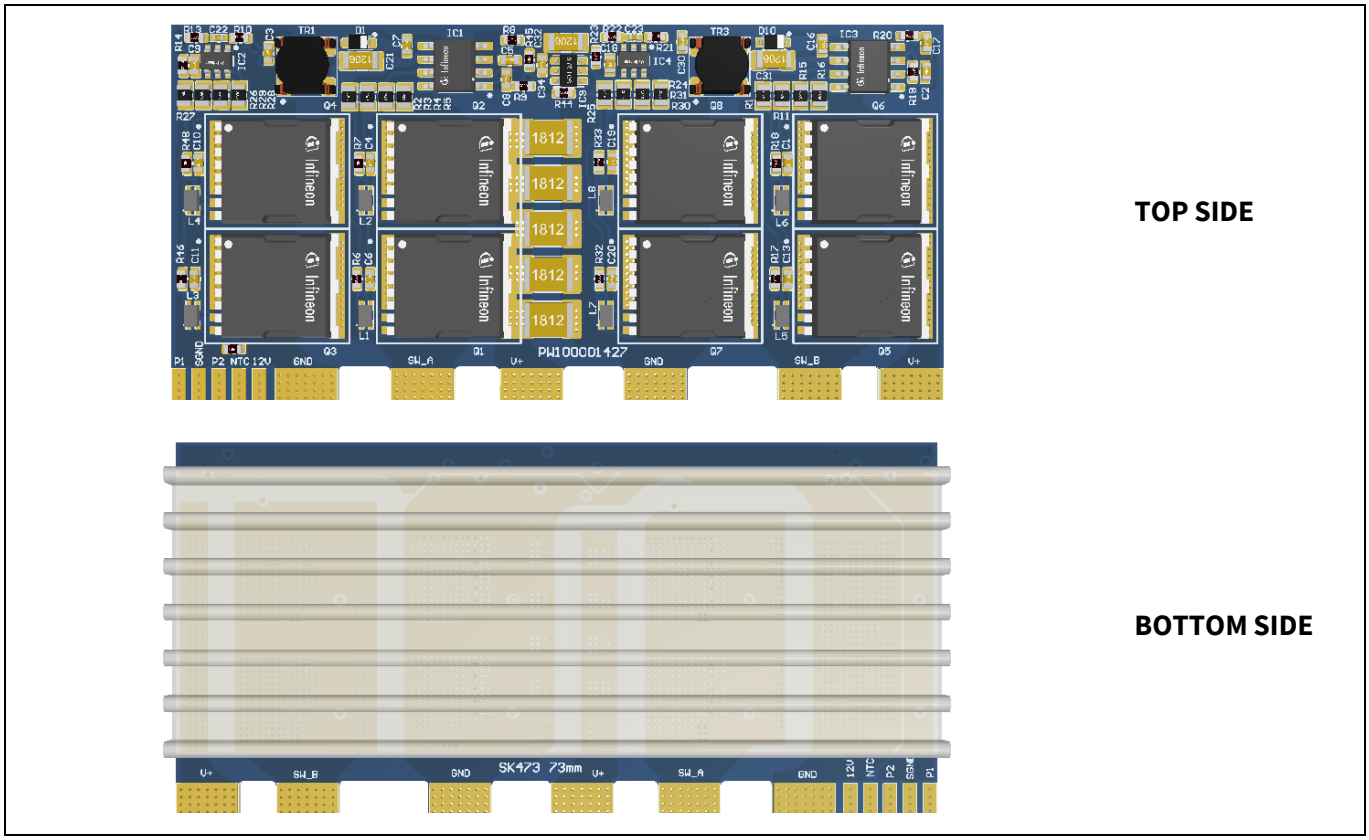


Figure 8 Overview of the LLC power daughter card

The PFC daughter card (PW200001428) integrates the two PFC stage bridges switching at 65 kHz, the synchronous rectification bridge, and a flyback converter that provides the 12 VDC (referred to primary) and the 5 V (referred to secondary) voltages. The driving supply for all the three bridges is done via bootstrap to keep the overall solution cost-effective.

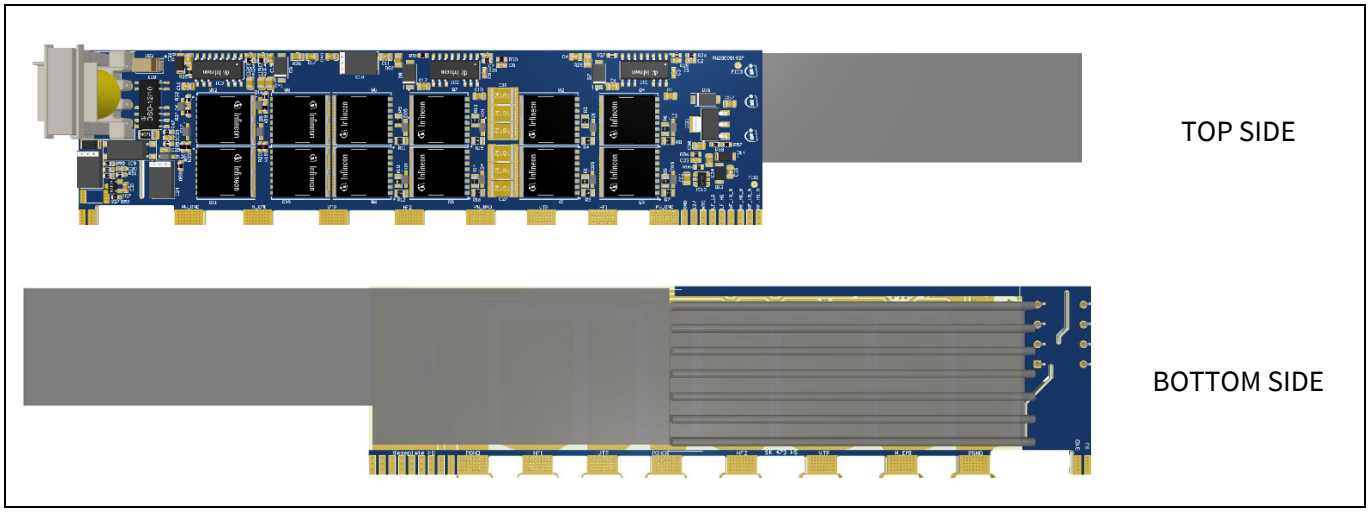


Figure 9 Overview of the PFC power daughter card

2.5.2 LLC transformer implementation overview

The LLC secondary side is embedded within two transformers having a planar structure, together with the LLC series resonant inductor and the parallel resonant inductor. Figure 10 shows a side view of the two transformers (XFMR A and XFMR B.) The code of the primary PCBs is MG500003085 and the secondary boards embedding the SR stage is MG100001429. More details about the topology, the driving scheme, and the control are presented in Section 3.2.

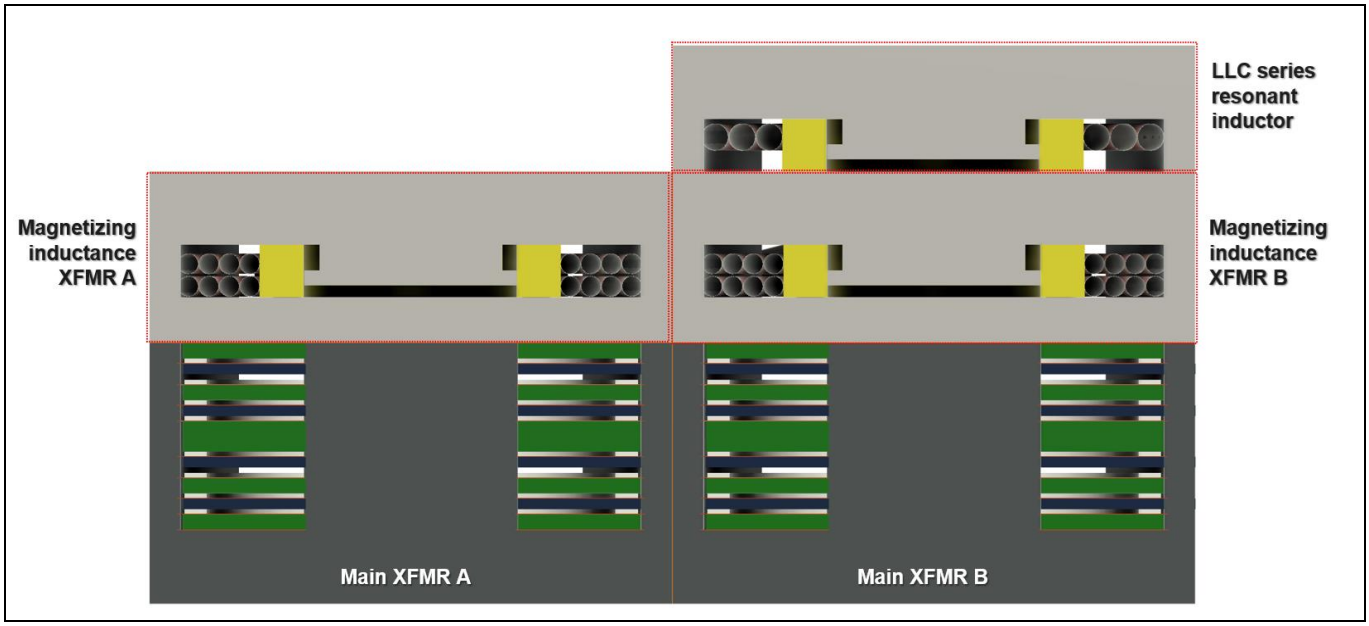


Figure 10 Overview of the LLC XFMR (transformer) structure

2.6 PSU efficiency and losses

The measured efficiency and the losses of the totem-pole PFC are shown in Figure 11 at different AC line voltages: 277 V_{AC}, 230 V_{AC}, and 180 V_{AC}.

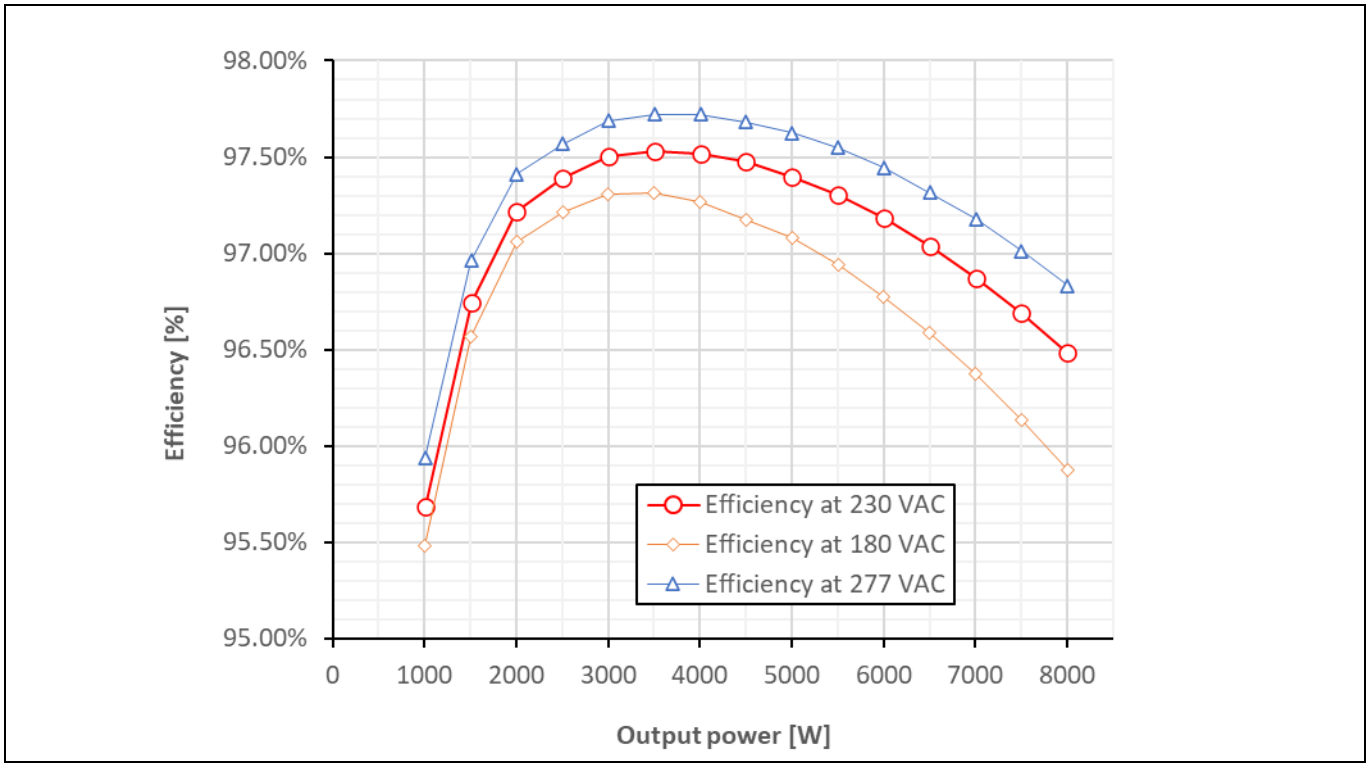


Figure 11 REF_8KW_HFHD_PSU's measured efficiency including fan power consumption

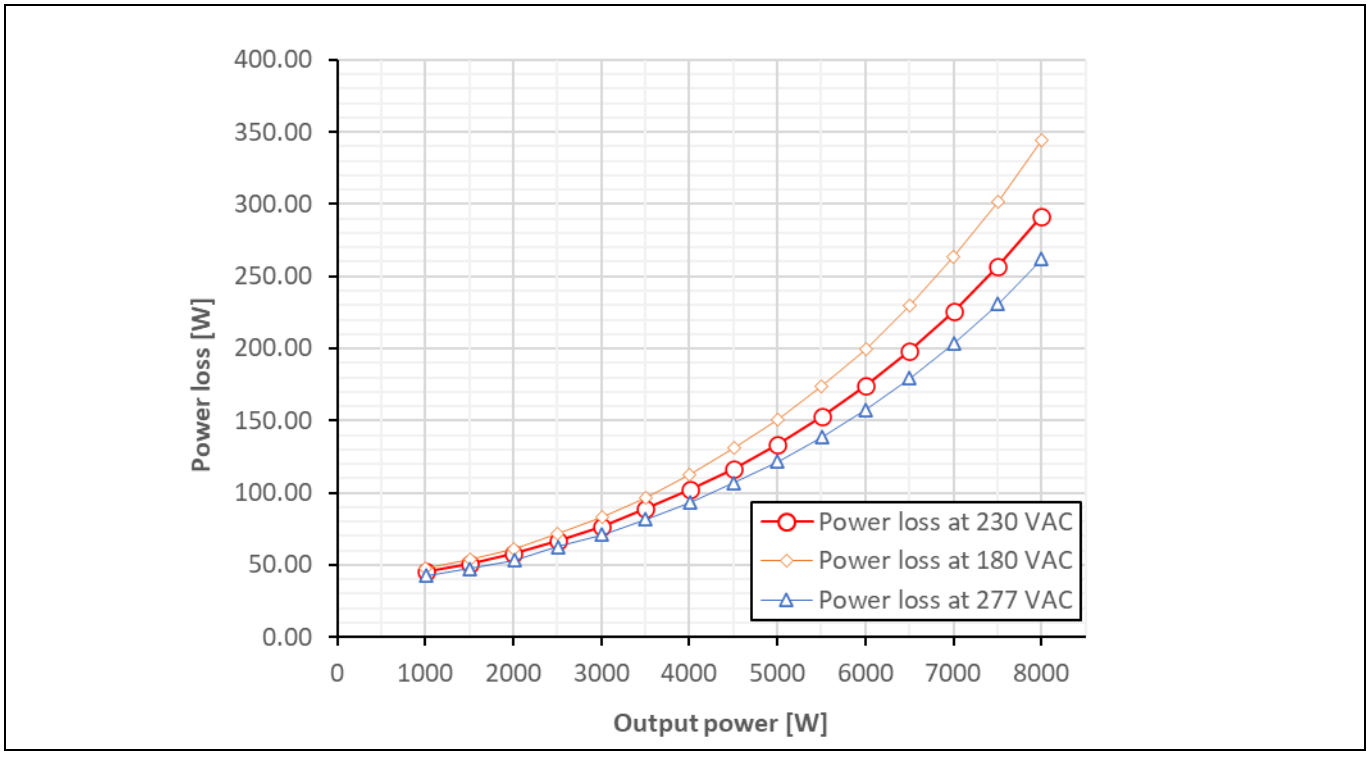


Figure 12 REF_8KW_HFHD_PSU's measured efficiency including fan power consumption

3 Topology blocks description

The operating principle of the bridgeless totem-pole PFC AC-DC and LLC DC-DC converter blocks shown in Figure 5 can be verified independently on Infineon's open-frame evaluation boards EVAL_3K3W_TP_PFC_SIC and EVAL_3K3W_LLC_HB_CFD7, available to order on the Infineon website or via distributors. Equivalent performance of the baby-boost circuit can also be evaluated on REF_3K3W_HFHD_PSU.

Note: In REF_8KW_HFHD_PSU, all the power circuits share power earth (PE) via the metallic chassis. For electrical safety and cooling reasons, it is recommended not to operate the board without chassis. It is the user's responsibility to ensure proper cooling and PE connections when operating the unit outside the chassis or out of the recommended operating conditions.

3.1 Bridgeless interleaved totem-pole PFC

3.1.1 Performance of the topology block standalone

A simplified schematic of the interleaved totem-pole PFC stage of REF_8KW_HFHD_PSU is shown in Figure 13.

The backplane power connector (i.e. TE 2391130-4 as per [1]) provides the AC input to the power supply unit, followed by the surge protection circuit and a two-stage input EMI filter. To support higher power density, the common mode EMI inductors of the EMI filter also integrate the differential mode inductance [2].

The filtered line AC input is connected to the two high-frequency CoolSiC™ fast-legs of the totem-pole PFC via filter-inductors ($Q_{A,HS}$, $Q_{A,LS}$, $Q_{B,HS}$, and $Q_{B,LS}$ in Figure 13), and neutral to the SR leg of the converter ($Q_{SR,HS}$ and $Q_{SR,LS}$ in Figure 13). The two high-frequency SiC bridges operate at 65 kHz switching frequency with interleaving, phase shifted by 180°, and the two SR legs rectify the AC current according to the detected line polarity (3.1.5).

Due to the high current stresses, all the PFC switches have two SiC MOSFETs in parallel to achieve lower equivalent $R_{DS(on)}$. Each switch of the unfolding bridge has two 10 mΩ Gen 2 CoolSiC™ devices in parallel, and each commutation slot in the fast-switching bridges has two 40 mΩ Gen 2 CoolSiC™ in parallel.

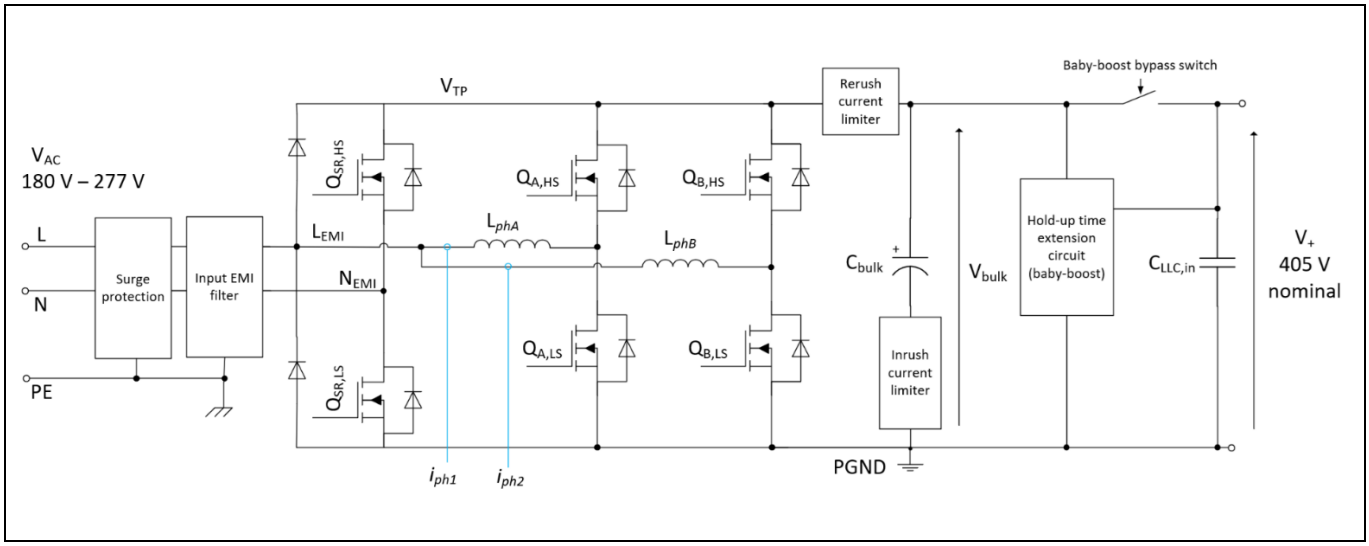


Figure 13 Simplified schematic of the PFC stage in REF_8KW_HFHD_PSU

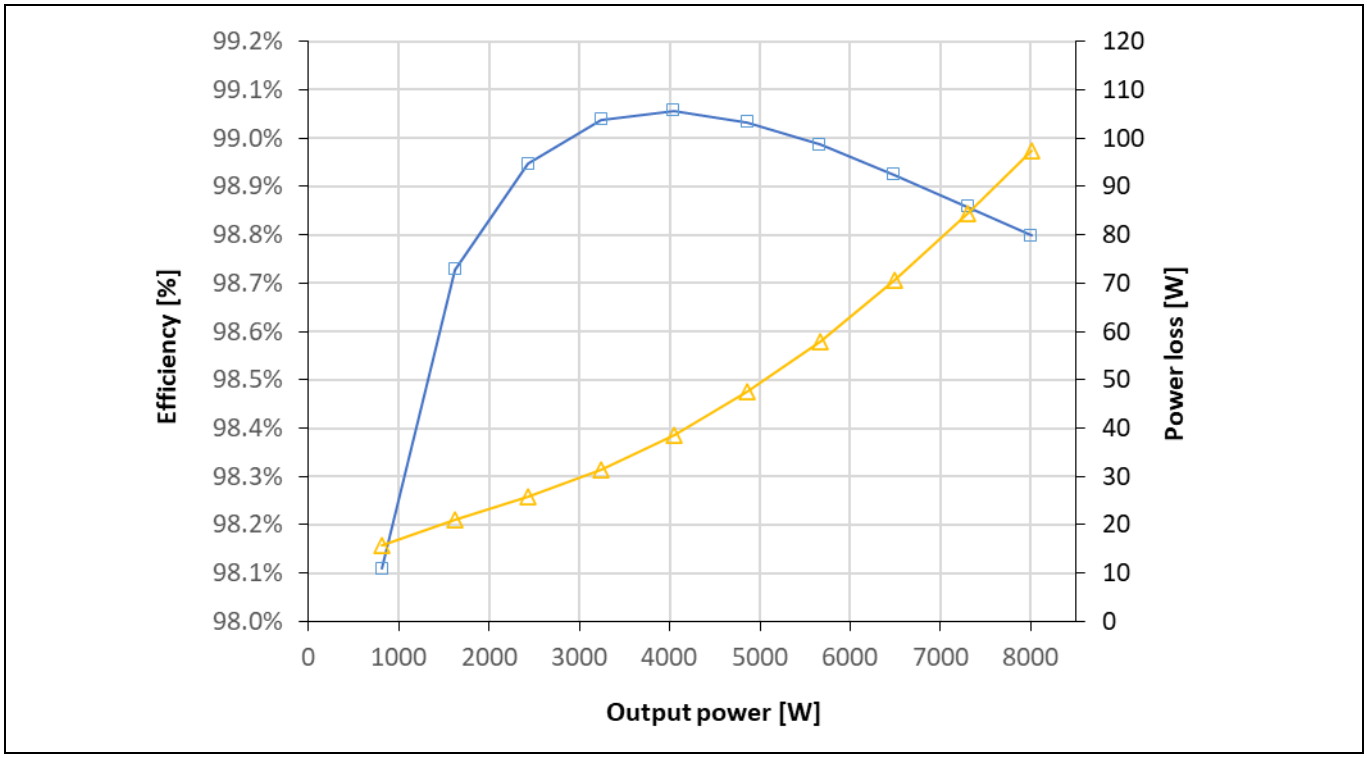


Figure 14 PFC efficiency and power losses standalone at 230 V AC input voltage

Figure 15 illustrates the distribution of losses among the PFC components at 230 V input AC voltage. The bar plot shows that the majority of the losses are related to conduction losses in the EMI filter and the PFC inductors, as well as bulk capacitor losses.

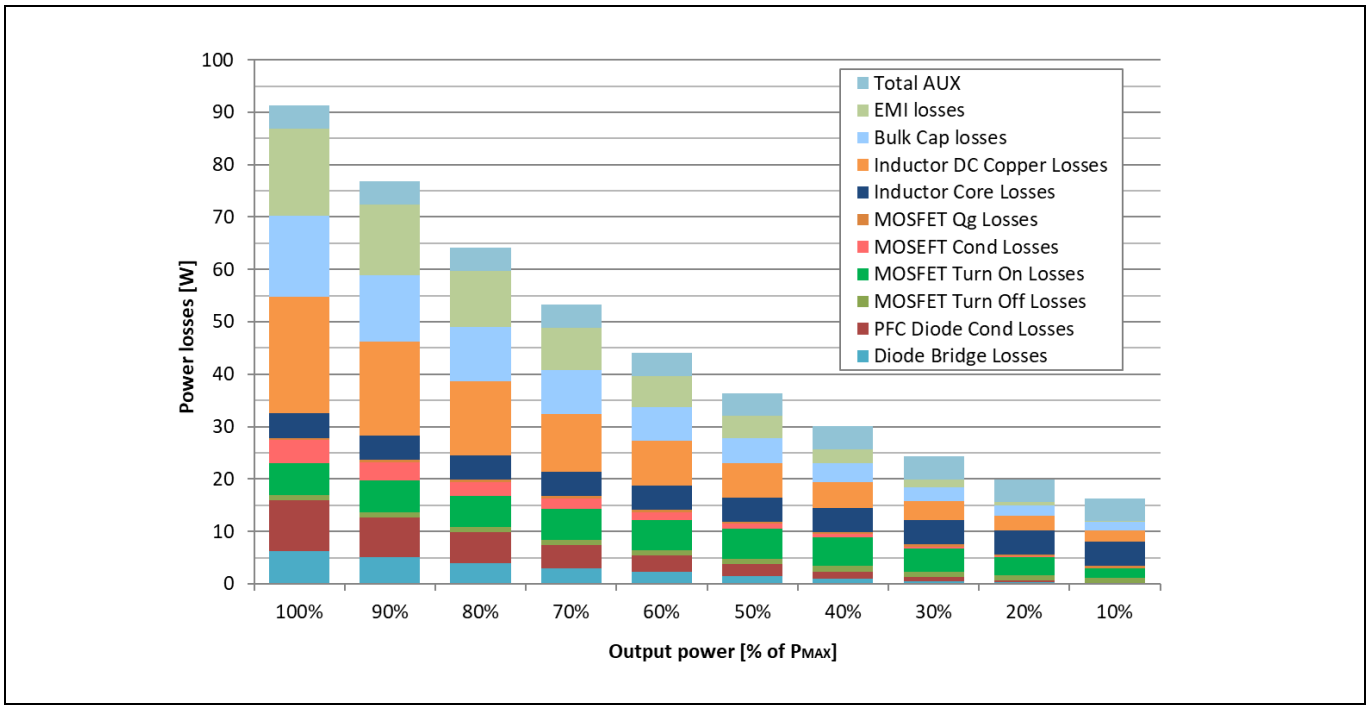


Figure 15 Breakdown of the PFC losses

3.1.2 EMI filter magnetics

The input EMI filter is a dual stage filter, where the two common mode inductors also integrate the differential mode inductance. The integration of the differential mode inductance is achieved by implementing a 0.3 mm magnetic shunt made of NO 30-16 electric steel. Each of the windings shown in Figure 17 (b) is made of flat copper wire, 0.6 mm × 6 mm, with N = 7 turns. With this arrangement, the estimated DC resistance of the EMI filter is ~4 mΩ per winding, resulting in a total resistance of ~8 mΩ at 25°C [2].

Two materials were investigated for constructing the input EMI filter chokes, the R10KC and the R5KZ from DMEGC. The R10KC has higher permeability resulting in higher self-inductance but lower resonance frequency, while the R5KZ has lower self-inductance but higher resonance frequency, therefore it keeps its inductive characteristics for a larger bandwidth. Eventually, R5KZ has been used for both the EMI integrated inductors with single magnetic shunt, as experimentally it has shown better performance in the EMI frequency range at the AC input (see Section 4.3).

In order to minimize the through hole sockets needed for the EMI filter inductor on the main board, a special winding arrangement has been used as depicted in Figure 17 and Figure 18. The combination of clockwise and counterclockwise winding (keeping the desired flux direction) allows combining four terminals into two.

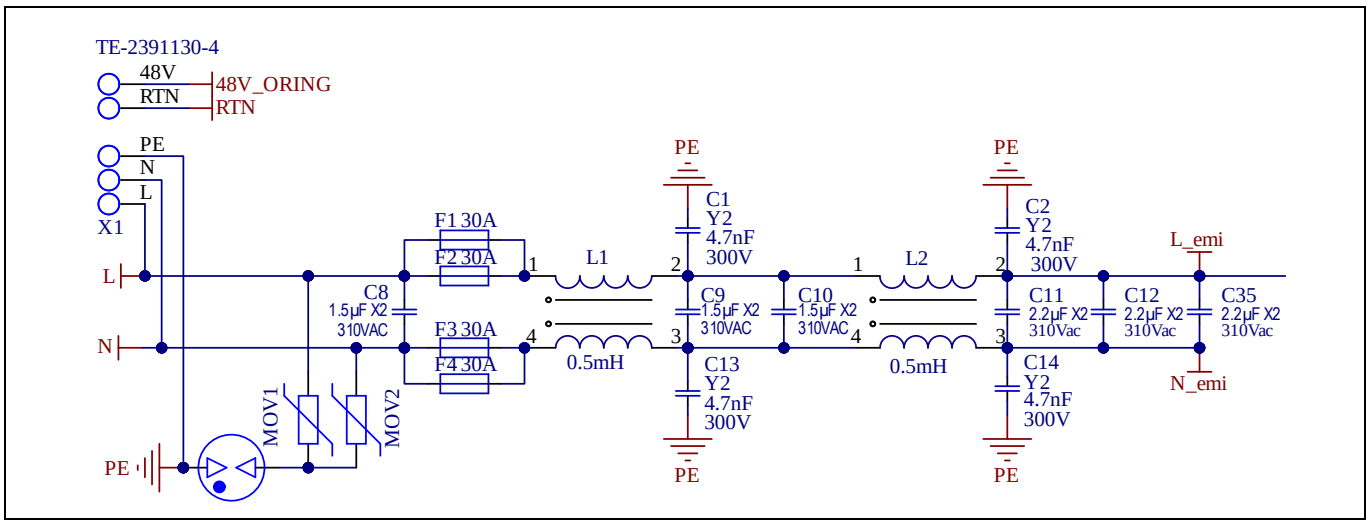


Figure 16 Schematic of the input EMI filter

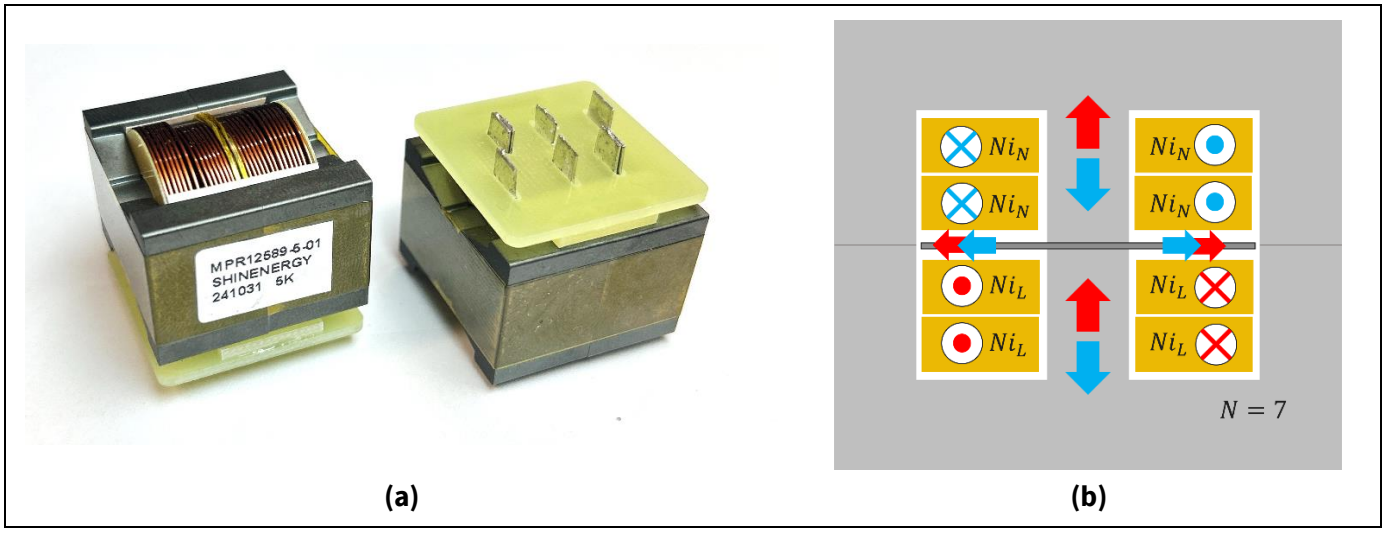


Figure 17 EMI input filter inductor (a) and differential flux direction (b)

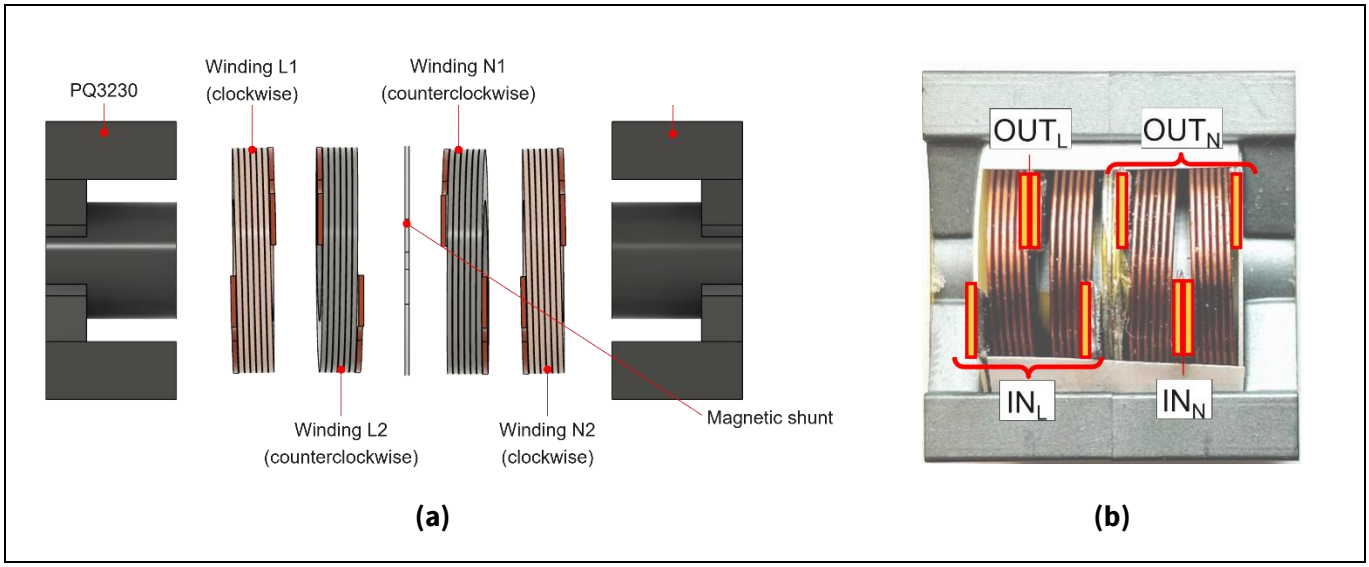


Figure 18 EMI common mode inductor details (a) and pinout (b)

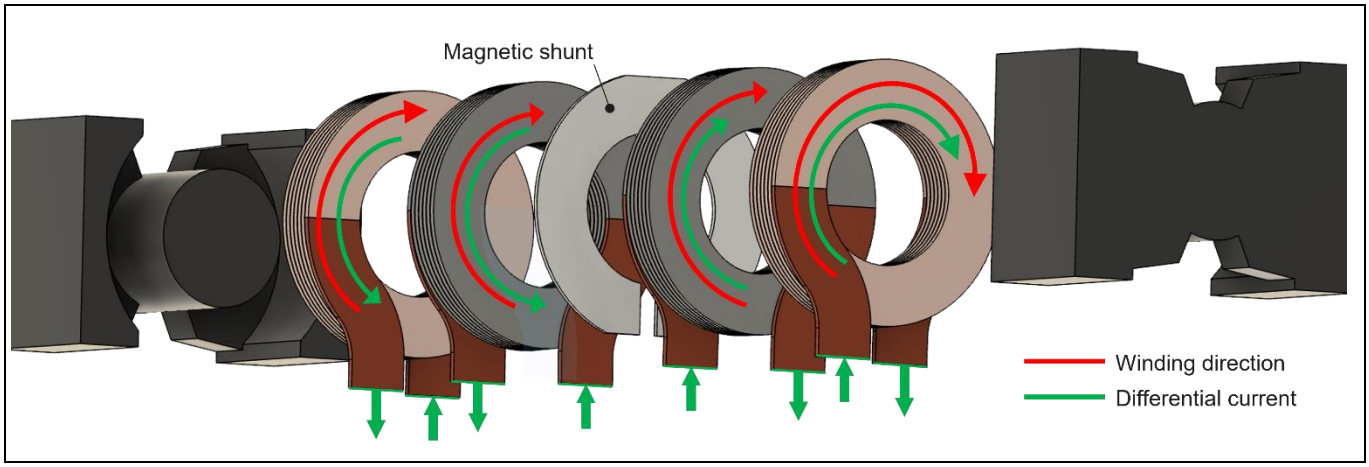
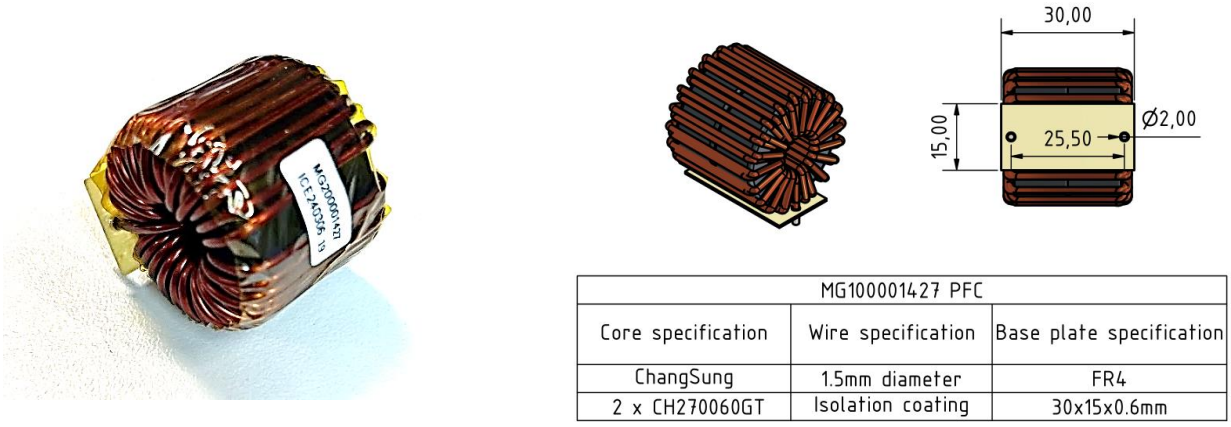


Figure 19 3D explosion drawing of the EMI filter inductor and a winding example

3.1.3 PFC magnetics

The PFC inductor choke design is based on a toroidal high-performance magnetic powder core. Toroidal chokes have a large surface area which allows homogeneous heat distribution without hot spots and allows good confinement of the magnetic field. In particular, in REF_8KW_HFHD_PSU, toroidal powder cores are used to limit stray magnetic fields (related to the low relative magnetic permeability of the core), as they can be coupled to the steel chassis and with the hall-effect current sensors of the PFC stages, resulting in a higher power loss and distorted phases and input currents. In the worst-case scenario at full load, it may affect the input current with the DC component super-imposed on the line frequency.

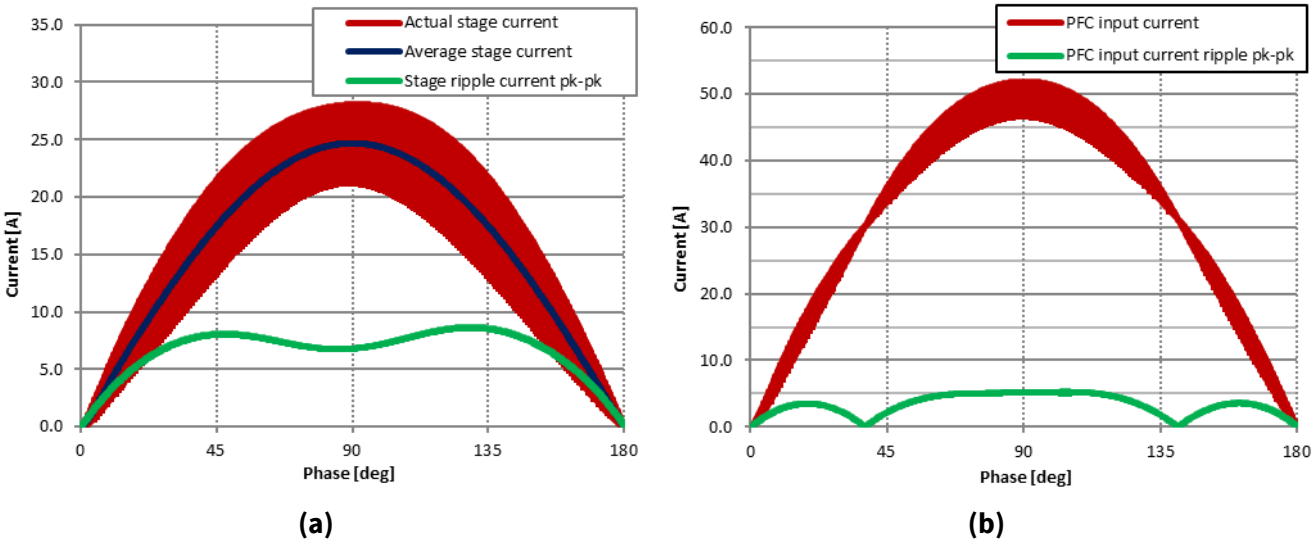
Each PFC inductor (MG200001427) uses two CH270060GT high flux GT cores from Chang Sung Corporation (CSC), which has an excellent DC bias and good core loss behavior. The winding is implemented using 39 turns of enameled AWG 15 (1.53 mm diameter) copper wire, double layer (see Figure 20). The inductance with no bias is 230 µH, and inductance in the presence of DC bias over one complete AC line cycle is shown in Figure 21.



MG100001427 PFC		
Core specification	Wire specification	Base plate specification
ChangSung	1.5mm diameter	FR4
2 x CH270060GT	Isolation coating	30x15x0.6mm

(a) (b)

Figure 20 PFC inductor picture (a) and specifications (b)



(a) (b)

Figure 21 Stage current (a), and input current at the totem-pole stage input (b) over a single AC line cycle at 230 V AC

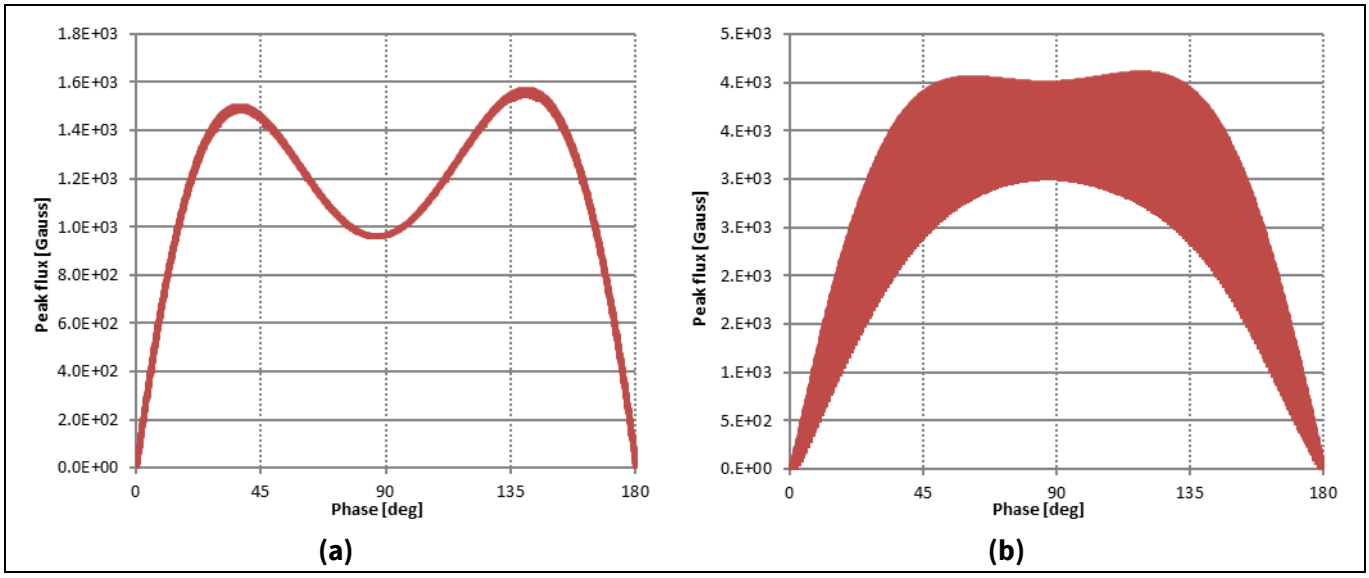


Figure 22 **Core high frequency flux (a), and total flux including AC line component (b) over a single AC line cycle at 230 V AC**

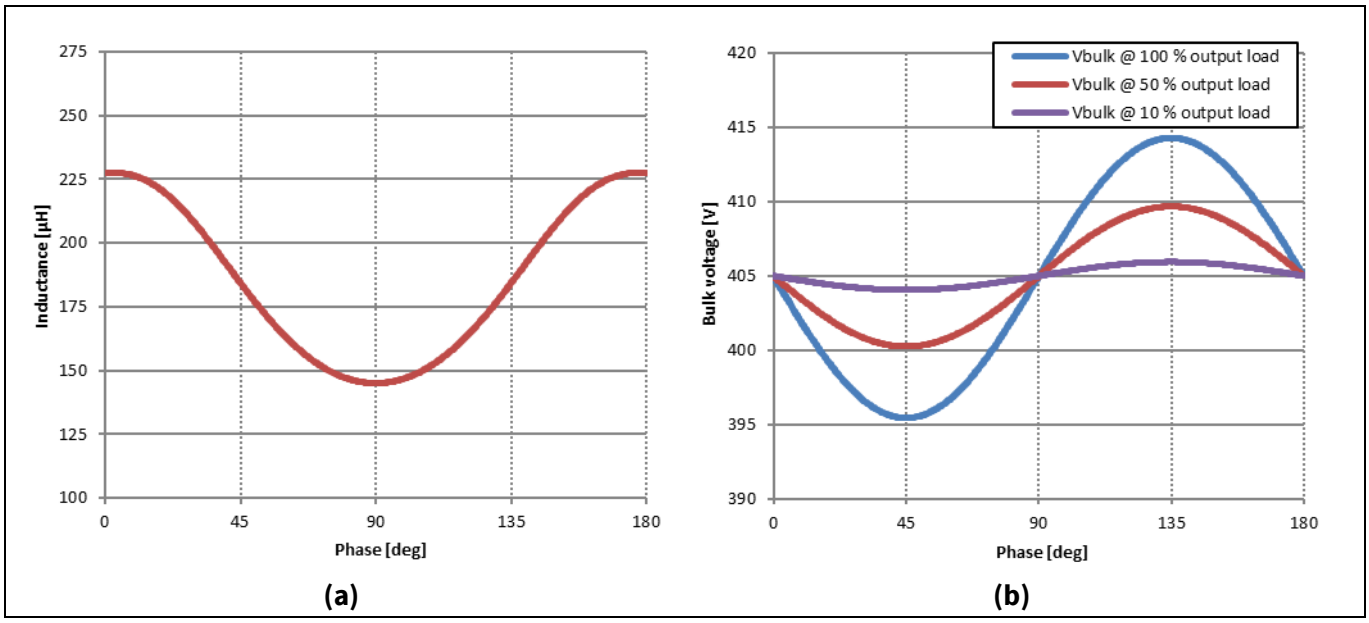


Figure 23 **PFC inductor effective inductance vs DC bias and bulk capacitance ripple over a single AC line cycle at 230 V AC**

3.1.4 Control scheme of the PFC

The two high-frequency bridges of the PFC stage of REF_8KW_HFHD_PSU are controlled in continuous conduction mode (CCM), and the currents through each of the two stages are monitored via hall-effect current sensors in series with the boost inductor. The currents through each of the two stages are then independently controlled with a two-loop approach, which operate based on the same current reference. The current loop is nested inside a low-frequency voltage loop (30 Hz bandwidth) for the regulation of the PFC output voltage to 405 V.

The overall control loop scheme includes feed-forward of the duty cycle (known the AC input and the bulk voltages) at the output of the current loop compensator, and a feed-forward of the LLC output load. The LLC load information is transferred from the LLC controller to the PFC XMC4200 controller via the UART interface.

Regarding the load feed-forward, information proportional to the PSU output current is added to the voltage compensator output to predict load jumps and have a faster reaction of the bulk voltage. This is needed, for example, during 0-100% load transients or vice versa, where the lower bulk capacitance for power density can cause the bulk to cross the OVP or UVP thresholds. Load feed-forward makes it possible to predict any PSU load change and have a fast reaction of the bulk voltage, independently of the voltage control bandwidth. Figure 24 shows the current loop (voltage compensator and sensing chains omitted) and how the two feed-forwards are implemented in it.

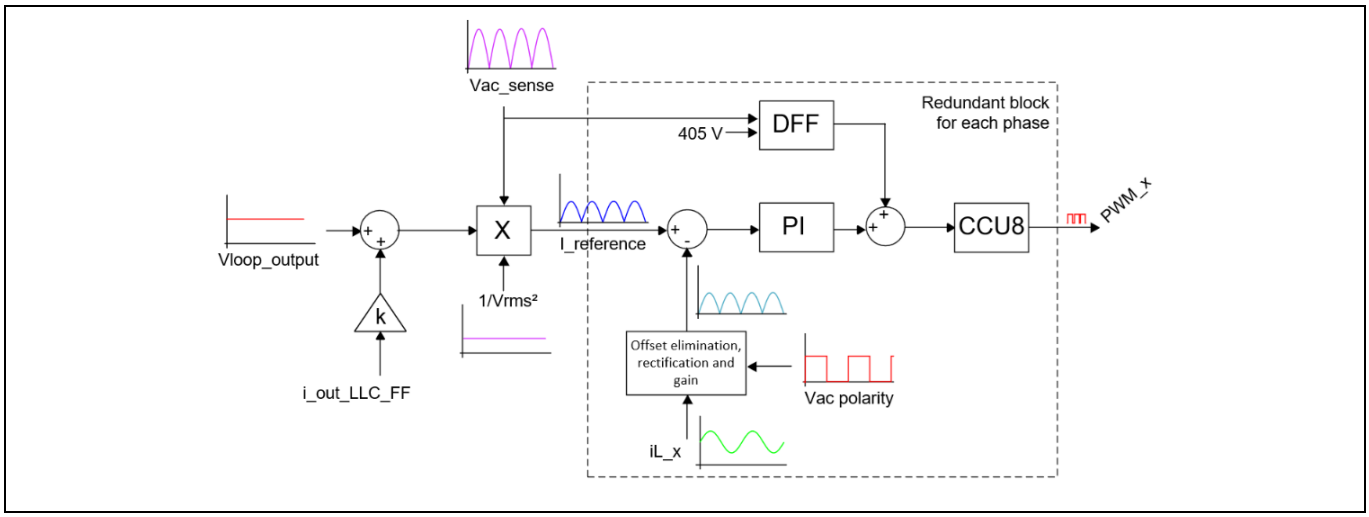


Figure 24 Current loop structure with details of load and duty-cycle feed-forward (DFF)

Duty feed forward (DFF) is applied by calculating the ratio of the AC sensed voltage to the reference voltage of the voltage loop.

To operate up to 277 V_{AC}, a dynamic increase of the voltage loop reference has been implemented to keep power factor correction operation. Indeed, the reduced amount of bulk capacitance in the system results in a larger double line frequency ripple on the bulk, closer to the AC input voltage peak value (391 V at 277 V_{AC} RMS). Therefore, the AC RMS input voltage is measured after the EMI filter, compared to preset thresholds (240 V_{AC} and 255 V_{AC} RMS), and the bulk reference voltage is increased accordingly (For more details see Section 4.2.3).

3.1.5 Sensing in the PFC converter

Figure 25 reports a simplified overview of the sensing chains of the PFC stage in REF_8KW_HFHD_PSU. The sensed variables are the input AC voltage (amplitude and polarity), the currents of the two boost stages, the voltage on the bulk capacitor (V_{bulk}) and the voltage at the LLC input (V_+) both referred to power ground (PGND).

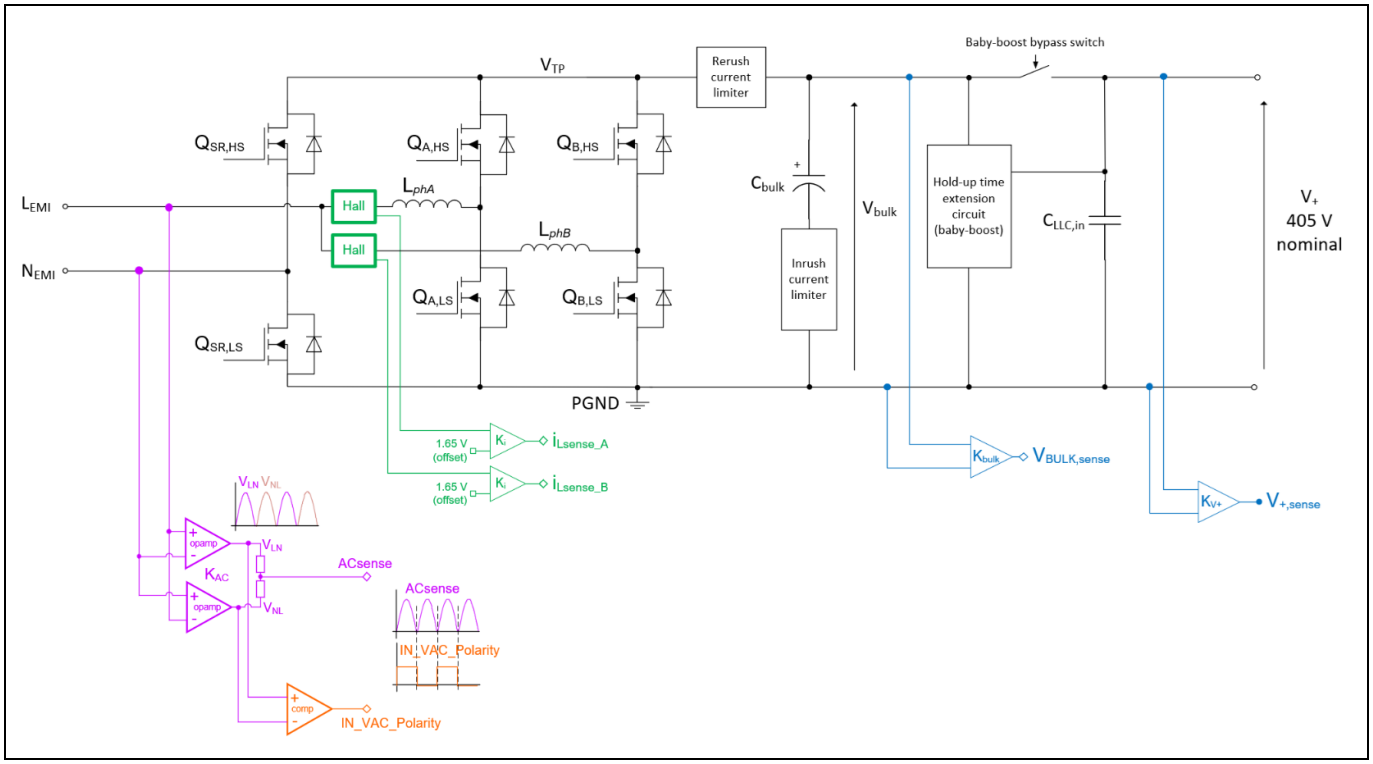


Figure 25 Sensing circuitry of the totem-pole PFC converter with XMC™

For the two boost currents, two hall-effect sensors have been used since they are a good fit for phase current sensing in the PFC stage. Indeed, unlike classic PFCs in which the AC voltage is rectified by the diode bridge, in bridgeless totem-pole PFC converters the inductor current can have both polarities. Furthermore, if the PFC controller ground is referred to the negative bulk rail, common-mode rejection is required to measure the inductor current. The analog output of the hall-effect sensor is biased with half of its supply voltage (i.e. V_{CC} = 3.3 V and V_{bias} = 1.65 V), thereby fitting the dynamic span of the sensor to the ADC input. To avoid DC offset, setting of the sensor output signals to auto-zero is done before the converter starts up by measuring the voltage at zero-current. In addition, considering that the sensor has enough bandwidth to sense the high-frequency ripple, the analog output can be used for peak-current limitation for each of the currents in the two stages.

The AC input voltage is sensed at the output of the EMI filter for noise reduction. The measurement is split into positive and negative AC sensing with respect to PGND, and the two resulting signals are then summed in the analog domain. Polarity detection of the AC input is obtained via comparator, shown in orange.

Finally, the bulk capacitor (V_{bulk}) and the voltage at the LLC input (V_+) are sensed via a resistive voltage divider with proper voltage scaling to comply with the analog-to-digital converter (ADC) input and the creepage requirements.

3.1.6 Driving CoolSiC™ and CoolMOS™ switches

CoolSiC™ Gen 2 switches have been used for all the active devices of the PFC converter. For CoolSiC™, a 19.5 V/0 V nominal unipolar bias voltage has been selected to minimize the $R_{DS(on)}$ of the switches.

Figure 26 shows an excerpt of the PFC schematic, detailing how to drive the 65 kHz switching bridge. Figure 27 shows the driving of the PFC rectifying bridge. For both the high-frequency and the low-frequency rectification bridges, a bootstrapping approach has been followed. This ensures a cost-effective and simple implementation on all the PFC bridges.

SiC MOSFETs have a positive temperature coefficient. Therefore, to lower the on-resistance, two devices per switch can be paralleled for every commutation slot in all the three PFC bridges. Further information on parallelization of SiC devices can be found in [3].

For obtaining the bias voltages, the 12 V_{DC} voltage from the flyback converter referred to PGND is first doubled to 24 V nominal, and then regulated to V_{reg} = 20.2 V by means of an LDO. The low-side switches are then supplied with V_{reg}- V_{FW} (V_{FW} is the forward voltage drop of the diode D15 in Figure 28 for bias voltage equalization), and the high-side switches are also bootstrapped starting from the same V_{reg} voltage. Bootstrap capacitance (3x 4.7 µF) has been increased for the LF leg to ensure enough energy to supply the I_{DD} quiescent current of the gate driver output chip for one entire AC line cycle.

Figure 29 reports the bootstrapped voltage of the high-side switch of both the high-frequency (stage A) and the low-frequency bridges measured on the PFC standalone. Stage B of the high-frequency bridge is not reported as having a similar voltage to stage A.

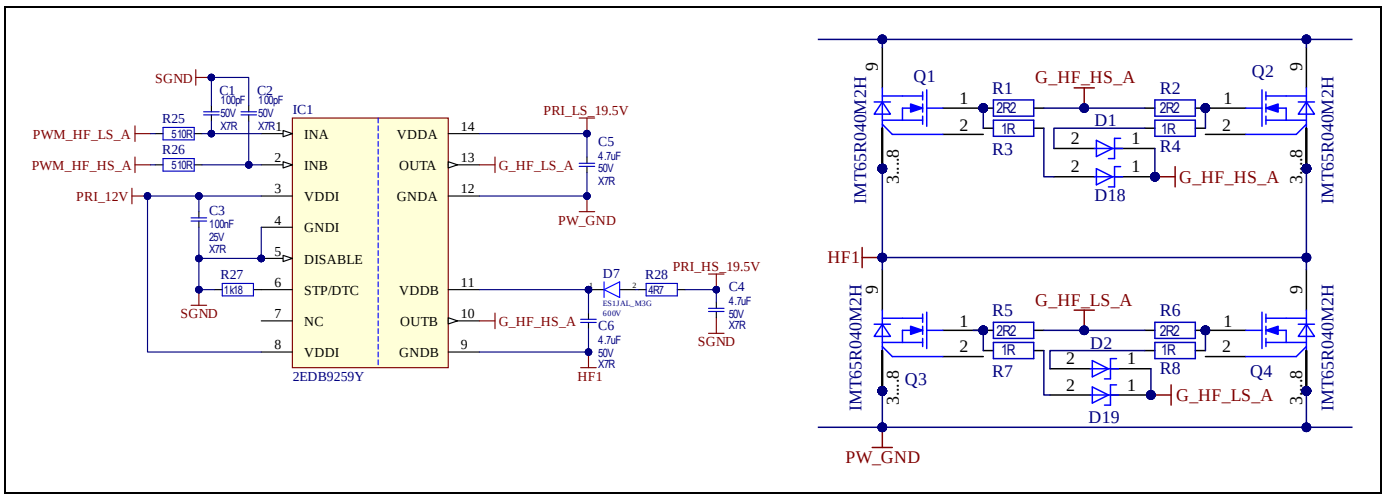


Figure 26 Driving CoolSiC™ in the fast-switching bridge

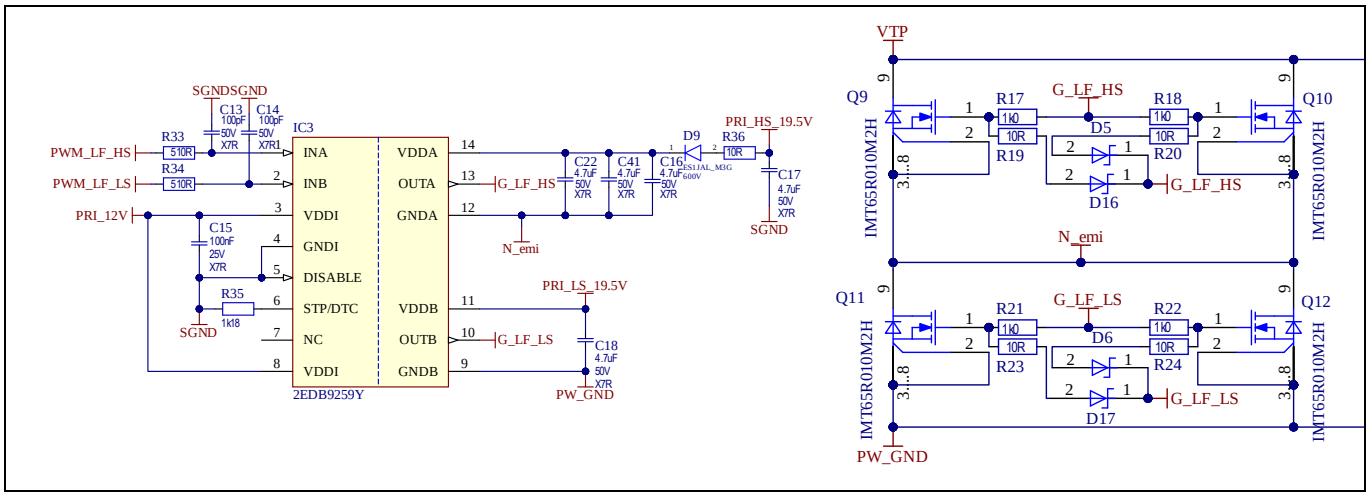


Figure 27 Driving CoolSiC™ in the rectification bridge

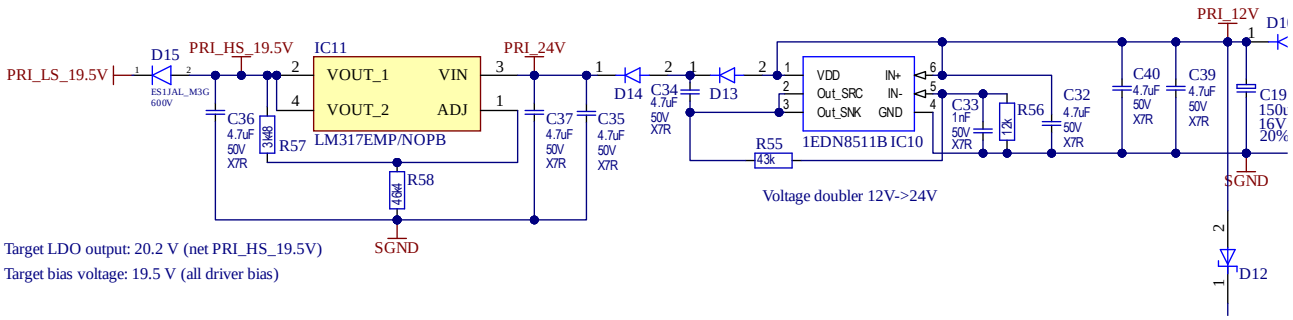


Figure 28 Regulated supply voltage for HF and LF bridges bootstrapping

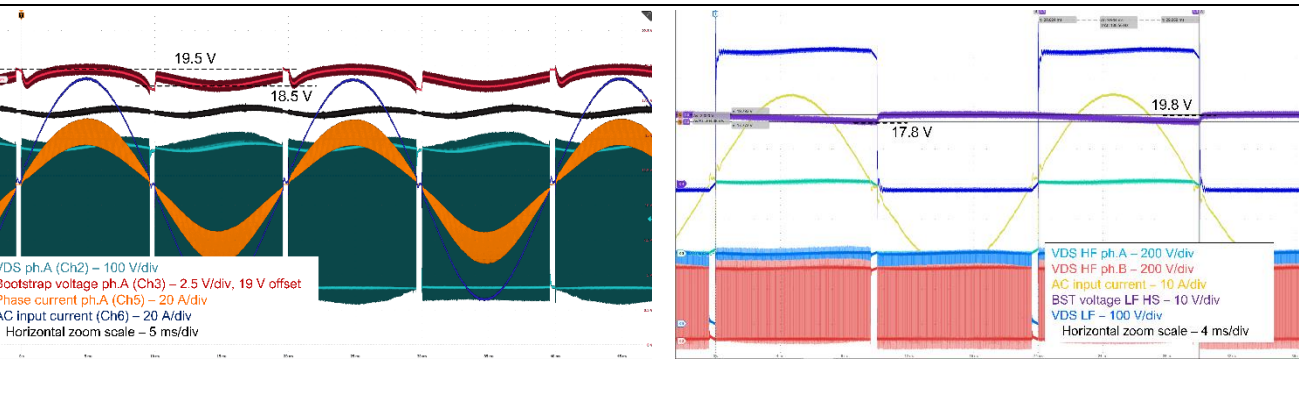


Figure 29 High side bootstrap capacitor voltage of the HF bridge – (a) Stage A (b) LF bridge, both during one AC line cycle

3.2 High frequency LLC resonant converter

One of the key elements to increase power density to 100 W/in^3 while keeping the highest possible efficiency is to reduce the volume of the high frequency transformer, by increasing the operating frequency of the DC/DC converter. A simplified schematic of the chosen topology is available in Figure 30.

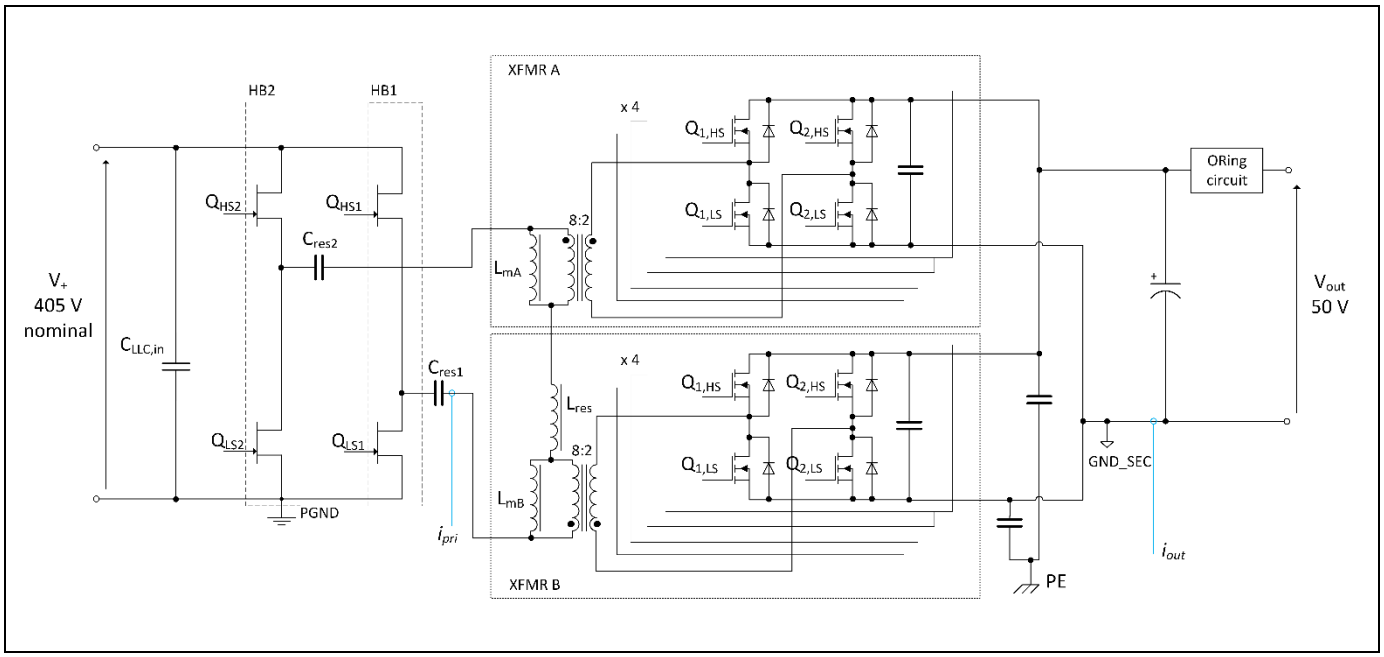


Figure 30 Simplified schematic of the LLC DC/DC converter in REF_8KW_HFHD_PSU

The primary full bridge (FB) of the LLC uses Infineon's CoolGaN™ technology to reduce driving losses, and is hosted on a dedicated daughter card on the main board as previously mentioned. The two resonant capacitors are on the main board, which also provide the connection path to the two high-frequency transformers. The primary full-bridge of the LLC then drives the two high-frequency transformers, configured as series input parallel output (SIPO).

Regarding the selected topology for the LLC converter, a configuration of series connected transformers was selected for two main reasons. The first reason is the distribution of the losses in the two magnetic structures instead of concentrating the power losses in a single transformer. The second reason is with the intention of achieving better EMI performance [4].

3.2.1 Performance of the standalone topology block

Figure 31 shows the measured efficiency of the half-bridge LLC converter, plotted for 405 V_{DC} input, which is also the nominal bulk voltage of the PSU. Efficiency is peaking at 98.7% at 50% of the rated load and remains above 98.2% from 25% to 100% of the rated output power.

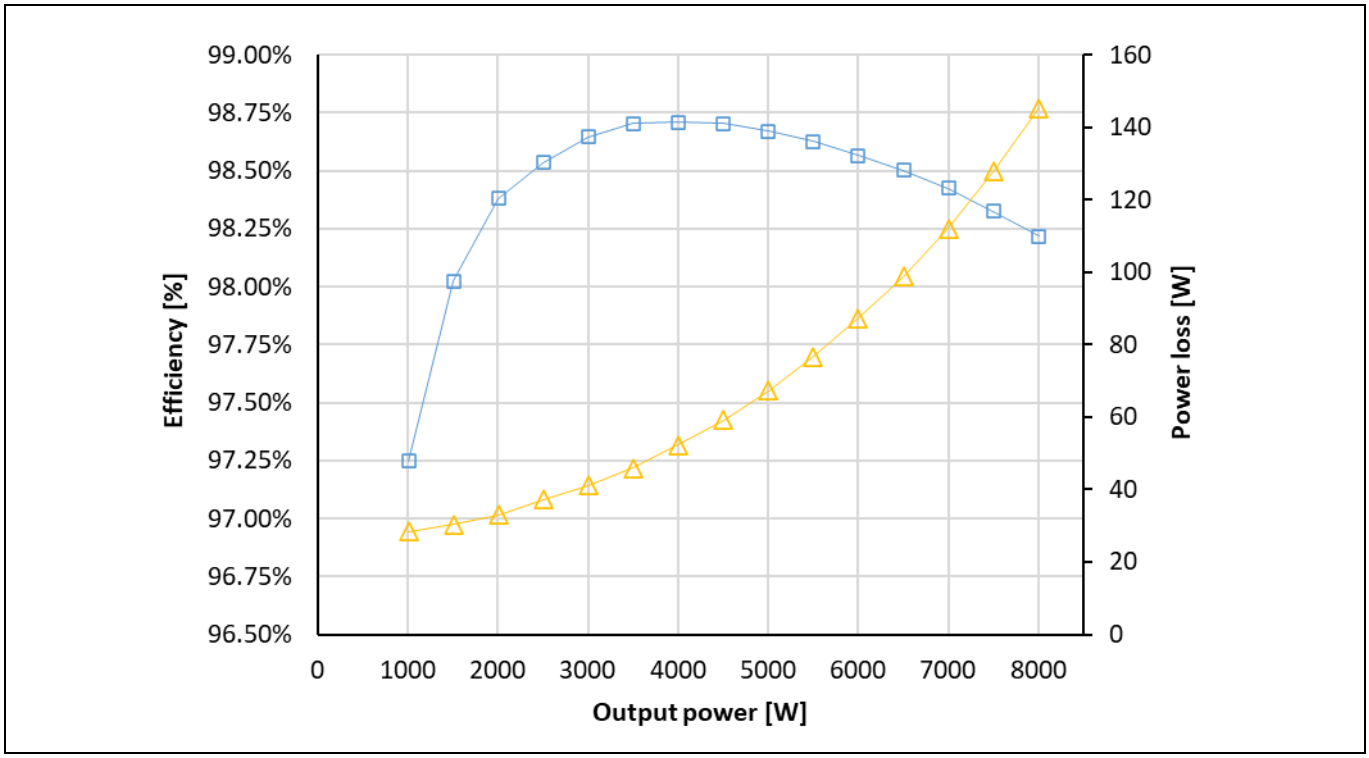


Figure 31 LLC DC/DC standalone: Efficiency and power losses at 400 V input

Figure 32 shows an estimation of the breakdown of the power losses for the LLC converter only. The main contributors to power losses are conduction losses of the primary side, the synchronous rectifiers, and total copper losses of the series and parallel inductance, and of the main transformer itself.

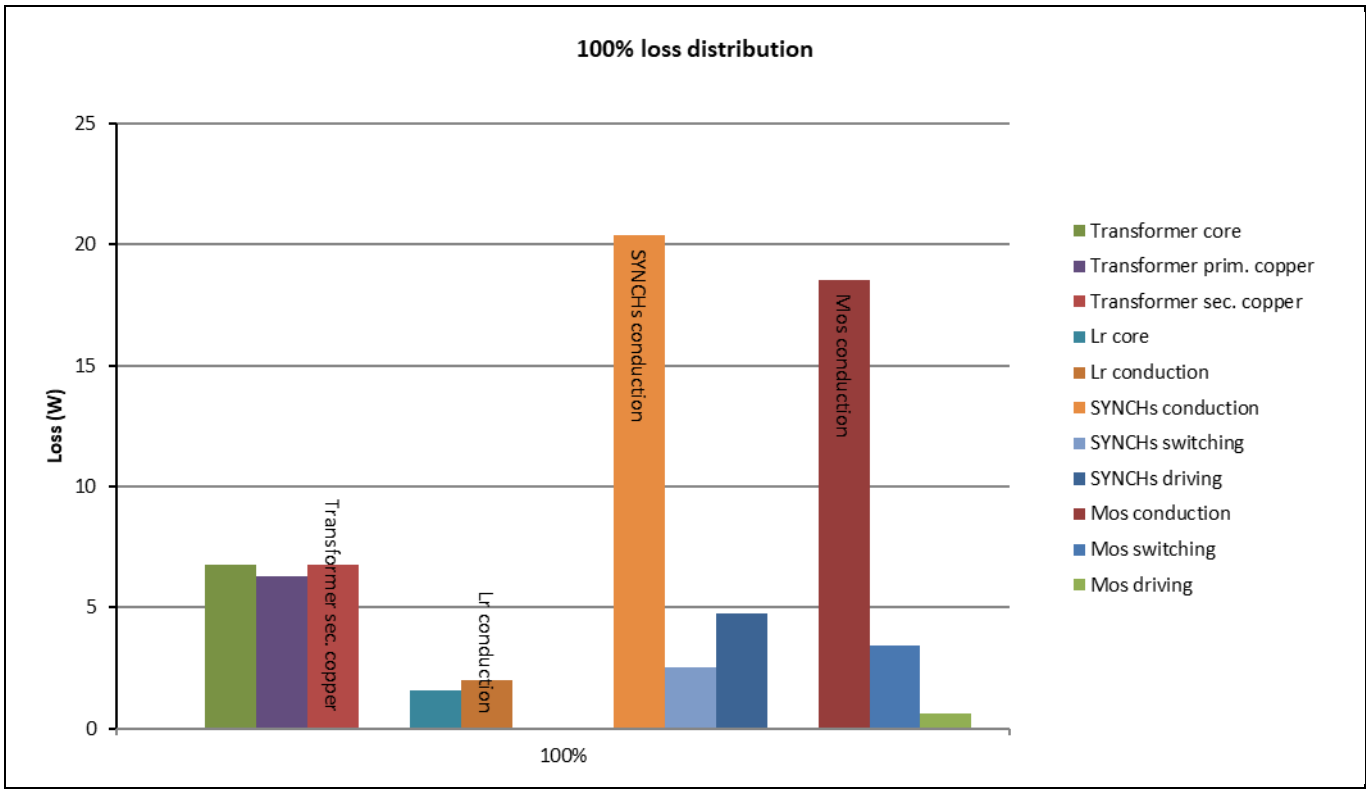


Figure 32 Power loss breakdown for the LLC DC-DC stage at 100% of rated power

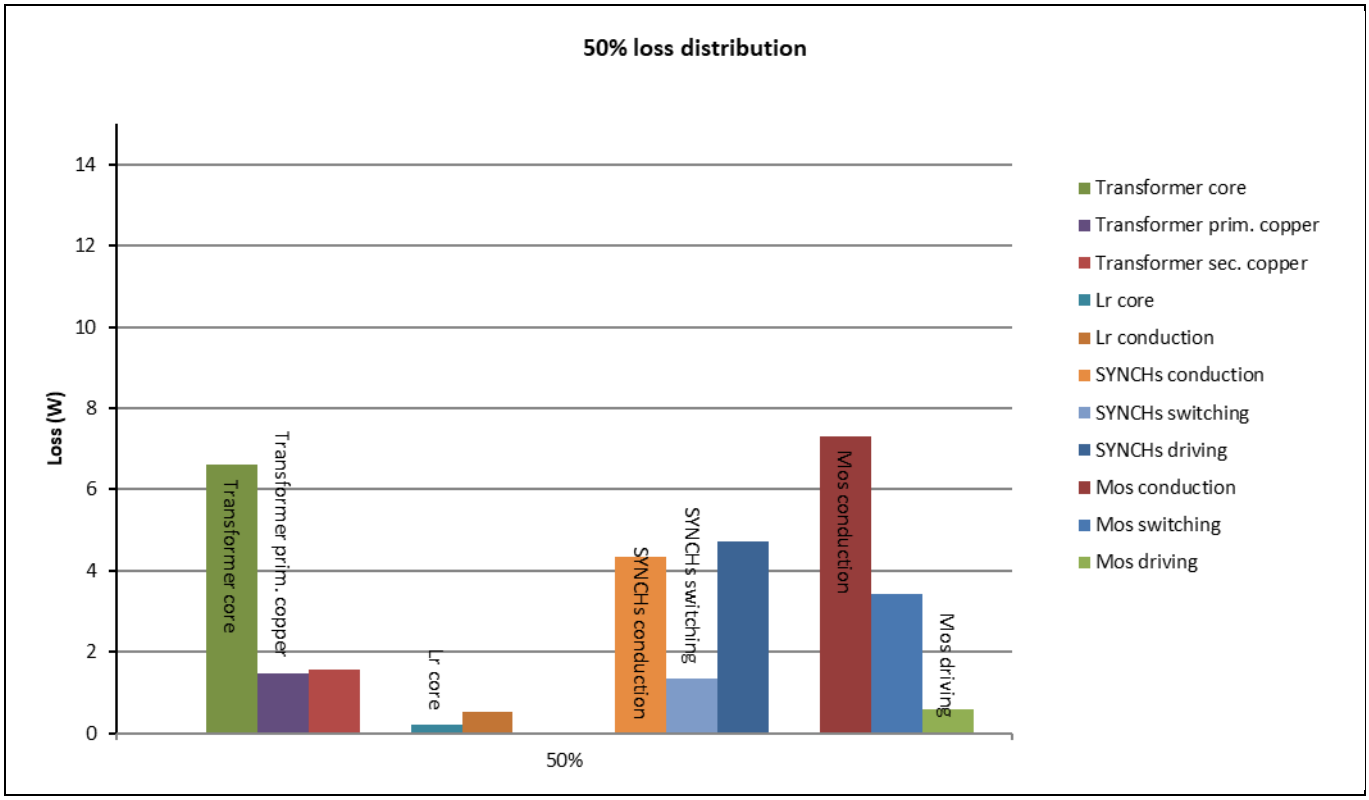


Figure 33 Power loss breakdown for the LLC DC-DC stage at 50% of rated power

3.2.2 LLC integrated transformer and inductors

Because of the height limitation of the PSU (40 mm), a cutout in the main board is made to accommodate the higher transformer (XFMR B shown in Figure 10), which is about 38 mm high, since it integrates both the series and the parallel resonant inductor of the LLC.

For both the transformers, several considerations have been implemented. First, with the aim of reducing the core losses, partial flux cancellation has been implemented for both the transformers. In the case of XFMR A, integrating one of the transformers and its parallel resonant inductors, partial flux cancellation occurs in the I-shaped core due to opposite flux directions generated by the transformer and the magnetizing inductance. In XFMR B, partial flux cancellation happens in the I-shaped core similar to XFMR A, plus a partial flux cancellation in the center column because of the interaction of the fields of Lm, Lr, and the transformer.

FR4 spacers are used between the primary and the secondary PCBs to reduce the primary-secondary interwinding capacitance. This benefits the EMI performance at the AC input, since reducing the interwinding capacitance allows to reduce the coupling of the high primary dV_{sw}/dt to the secondary side and therefore the coupling to the PE terminal through the LLC output Y-caps. Since PE is also connected to the AC input via the input side Y-caps, this results in EMI improvement at the AC input. Secondly, the lower interwinding capacitance also reduces the overall capacitance connected to the LLC primary switching nodes, enabling a larger ZVS operation range.

For the series connection of the two transformers, the series resonant LLC inductor is placed between the two XFMRs to make the impedance symmetrical as seen by the two high voltage bridges of the LLC primary side.

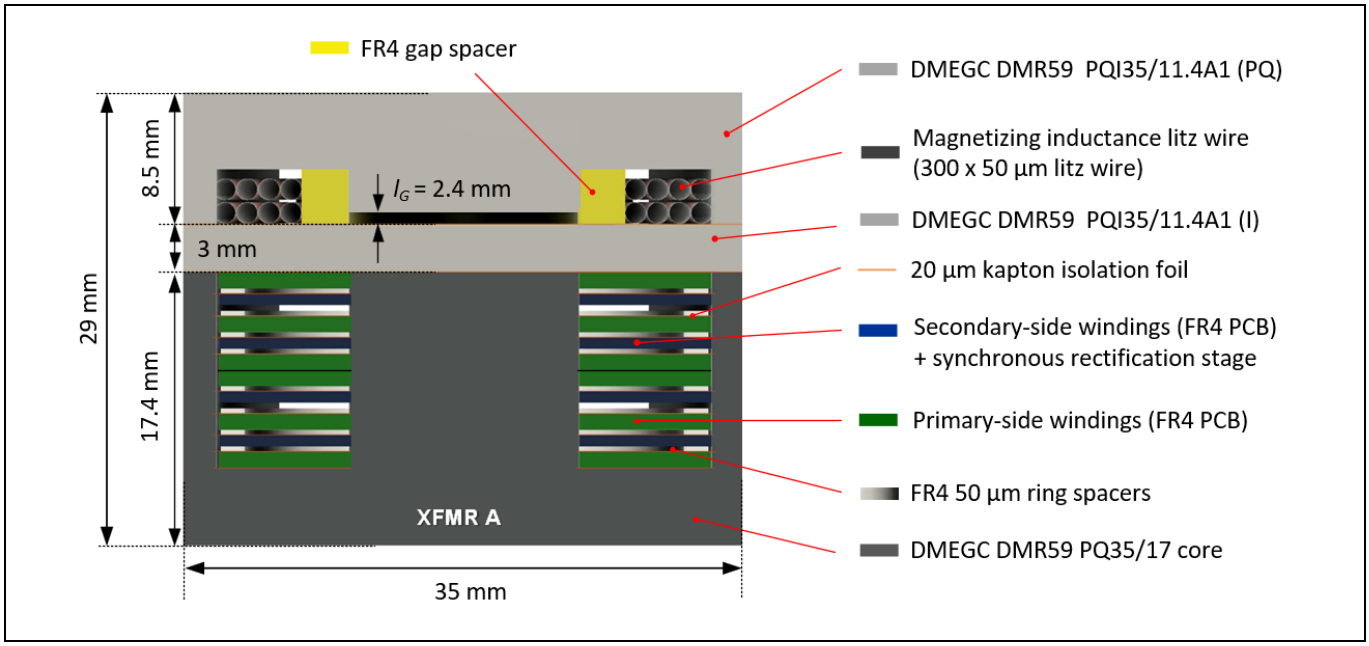


Figure 34 Detailed stack-up of XFMR A (transformer and parallel resonant inductor B integrated)

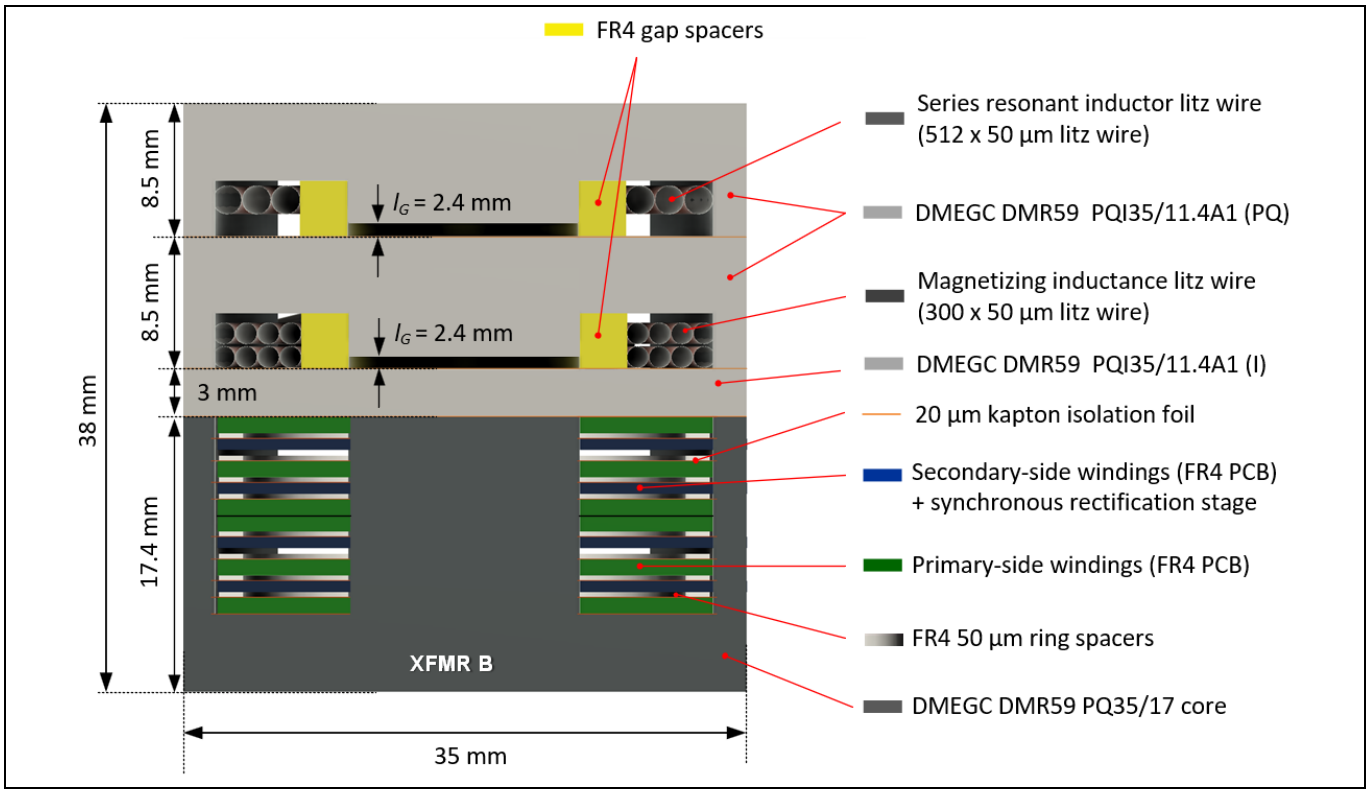


Figure 35 Detailed stack-up of XFMR B (transformer, series, and parallel resonant inductors A integrated)

The two XFMRs have dimensions of 35 mm × 29 mm × 50 mm and 35 mm × 38 mm × 50 mm respectively, including primary and secondary PCBs. DMR59 from DMEGC cores have been used since they offer lower core losses. For each of the main transformers, a stack with six primary and four secondary PCBs are used to achieve the desired turn ratio. All the secondary PCBs are in parallel, while the primary PCBs are in a 3+3 arrangement,

meaning there are two sets of three primary boards. In each set, the three primary boards are in parallel, and the resulting two sets are arranged in series.

Considering that each primary board realizes four turns and each secondary realizes two turns, this arrangement allows to realize an 8:2 turn ratio for each of the two transformers, resulting in a 16:2 turn ratio when XFMR A and XFMR B are in series on the main board. It is important to notice that four secondary PCBs for each transformer have been used, since this turned out to be the stack-up allowing the best copper utilization on the secondary side. Indeed, an additional secondary side PCB would have needed a change in the stack-up with the secondaries as outer boards, resulting in low copper utilization on the two most outer layers.

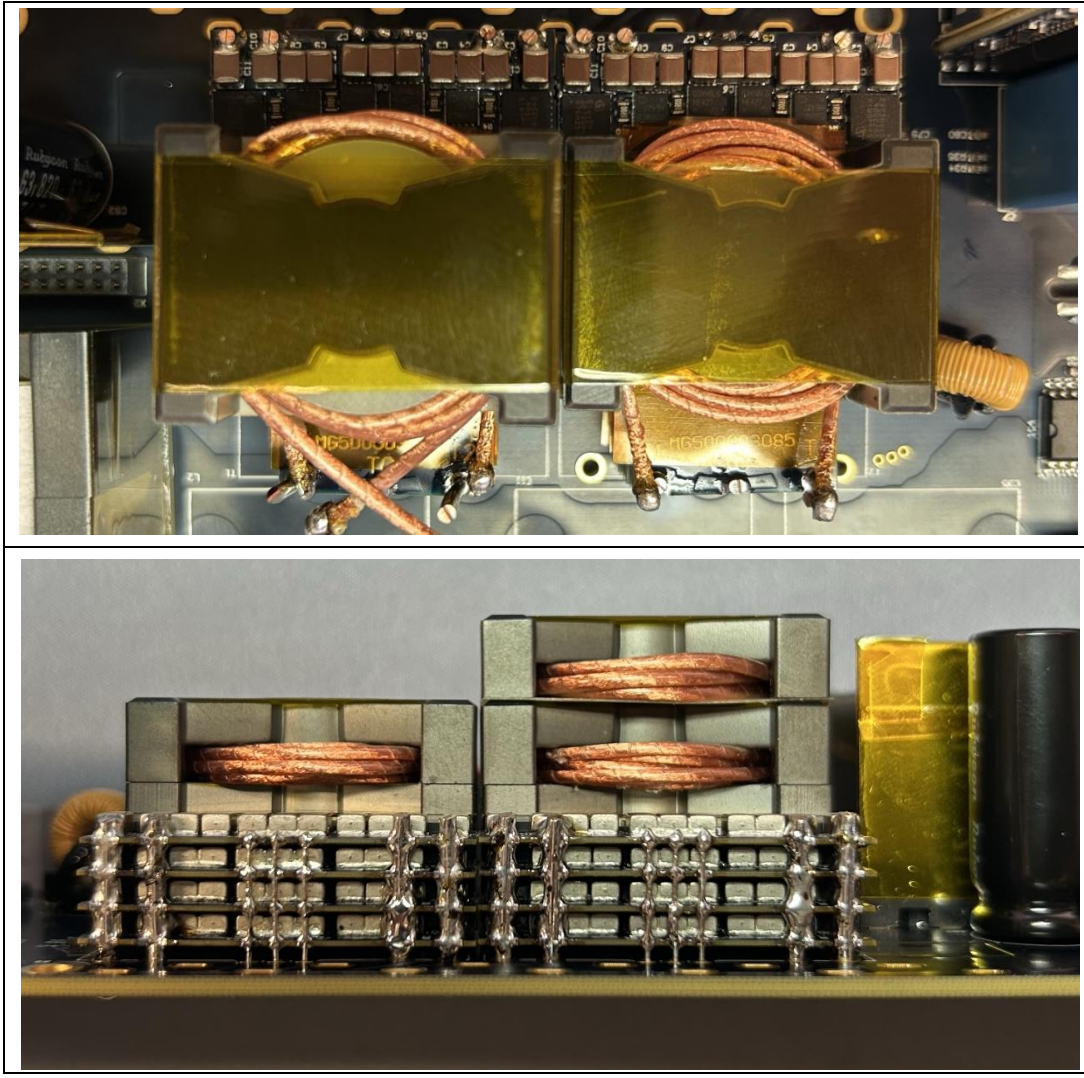


Figure 36 Integrated planar transformer assembly: Top view (a) and side view (b)

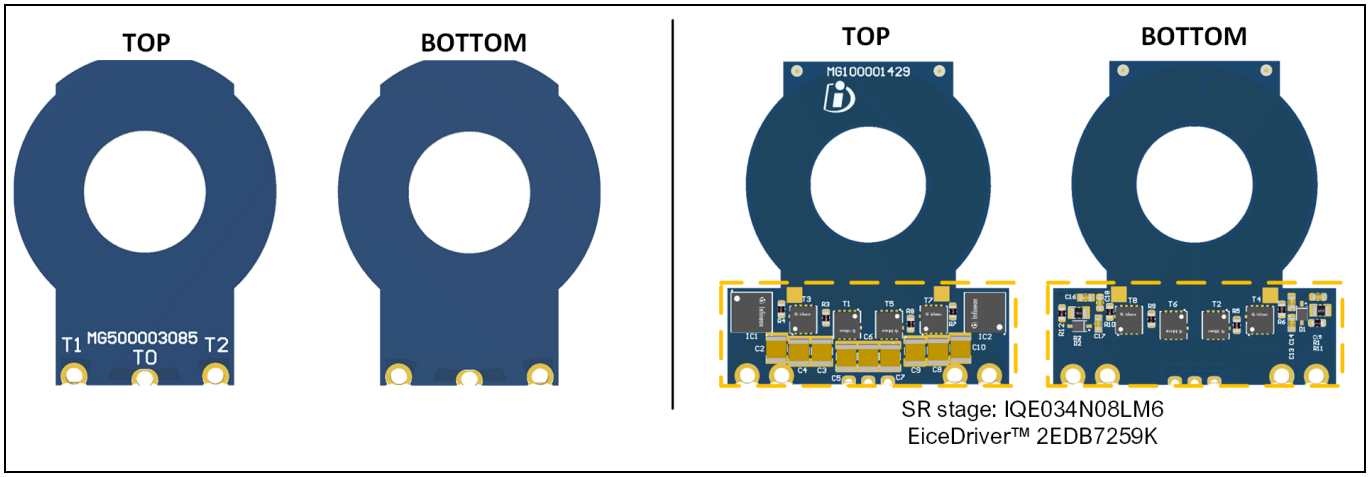


Figure 37 An overview of the primary- and secondary-side winding PCBs

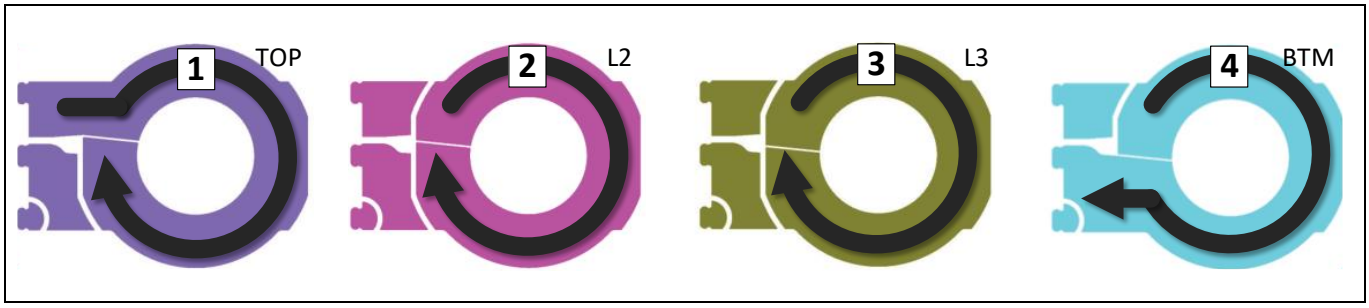


Figure 38 Detail of the primary side PCB: Winding arrangement for each board

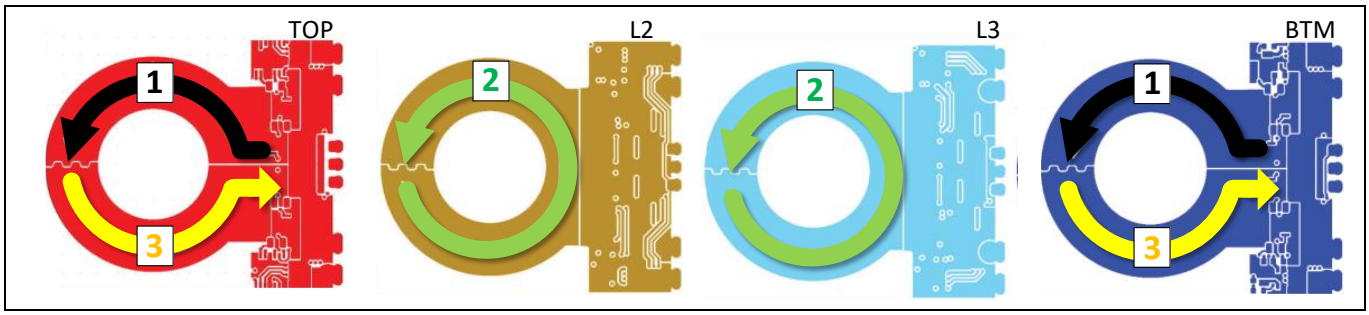


Figure 39 Detail of the secondary side PCB: Winding arrangement for each board

3.2.3 Driving CoolGaN™ and OptiMOS™ switches

The primary side of the LLC converter uses four CoolGaN™ GIT devices, each having a 35 mΩ on-resistance in TOLL package (CoolGaN™ IGT65R035D2), with both high- and low-sides having two devices in parallel. To drive the CoolGaN™ devices efficiently with paralleling, a common mode (CM) choke is suggested in series with the gate-loop to increase CM impedance without affecting the differential mode (DM) impedances, which could affect the driving loop. For this purpose, four CM chokes from Bourns (SRF2012-361YA) have been used, as shown in Figure 40. Figure 41 shows a possible cost-effective approach for biasing the high-side drivers having low interwinding capacitance. For further information on GaN paralleling, see [5].

Low-side drivers are interlocked via PWM inputs to protect them from potential cross-conduction in the GaN high voltage bridges. On the secondary side, the same is achieved by using the internal dead-time control (DTC) of the driver (see Figure 42).

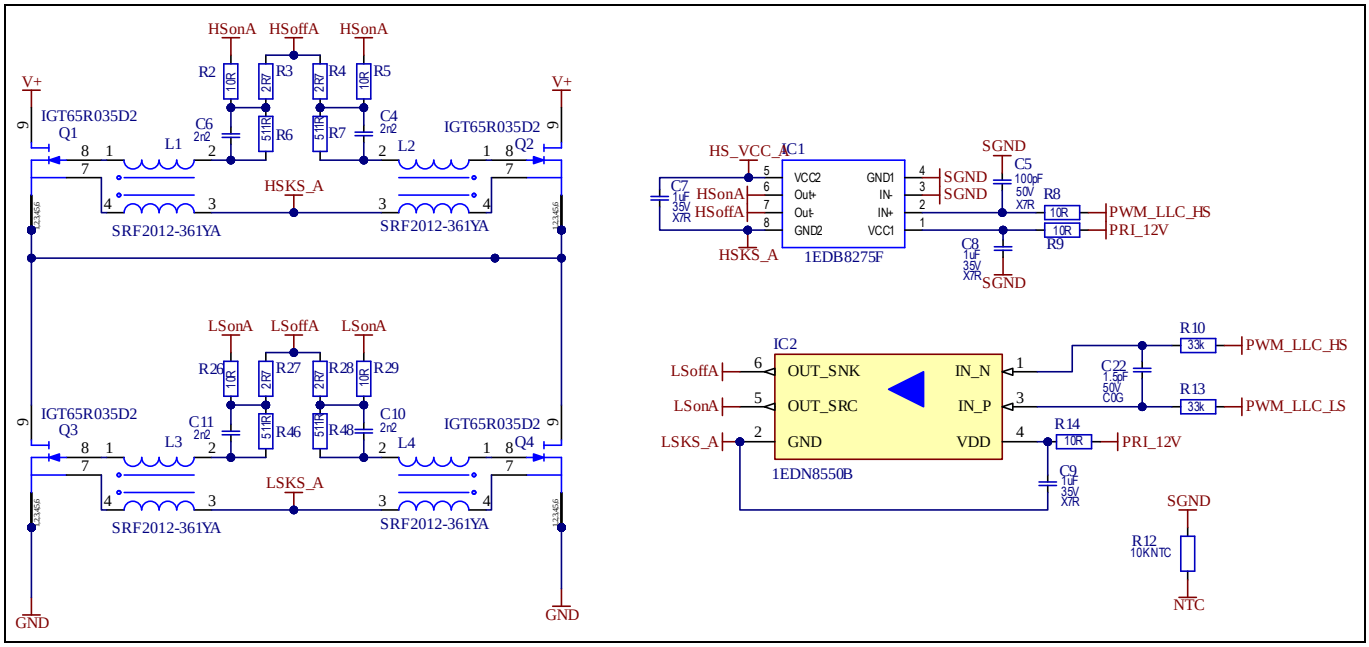


Figure 40 Driving CoolGaN™ on the primary side of the LLC converter

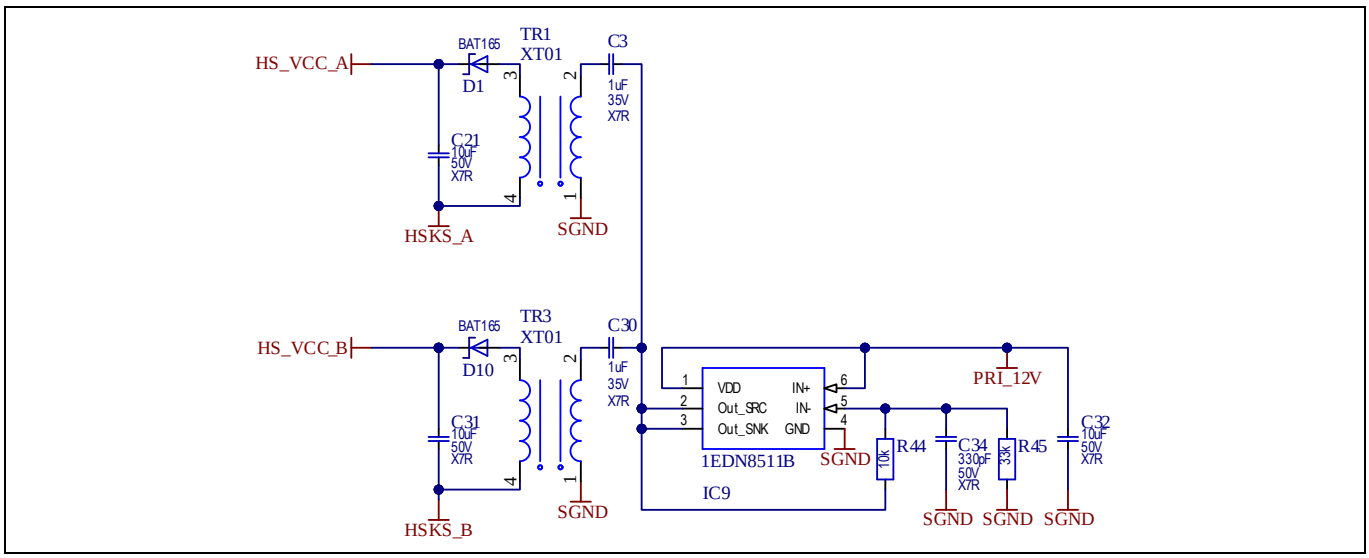


Figure 41 Biasing of the high-side driver for CoolGaN™ driving

For the bias supply of the OptiMOS™ MOSFETs on the secondary side, a bootstrapped solution with a 5 V_{DC} bias is used as shown in Figure 42. Because of the space constraints, EiceDRIVER™ 2EDB7275K in a 5 mm × 5 mm package is used, which fits the small space available on the secondary board stacked in the transformer structure.

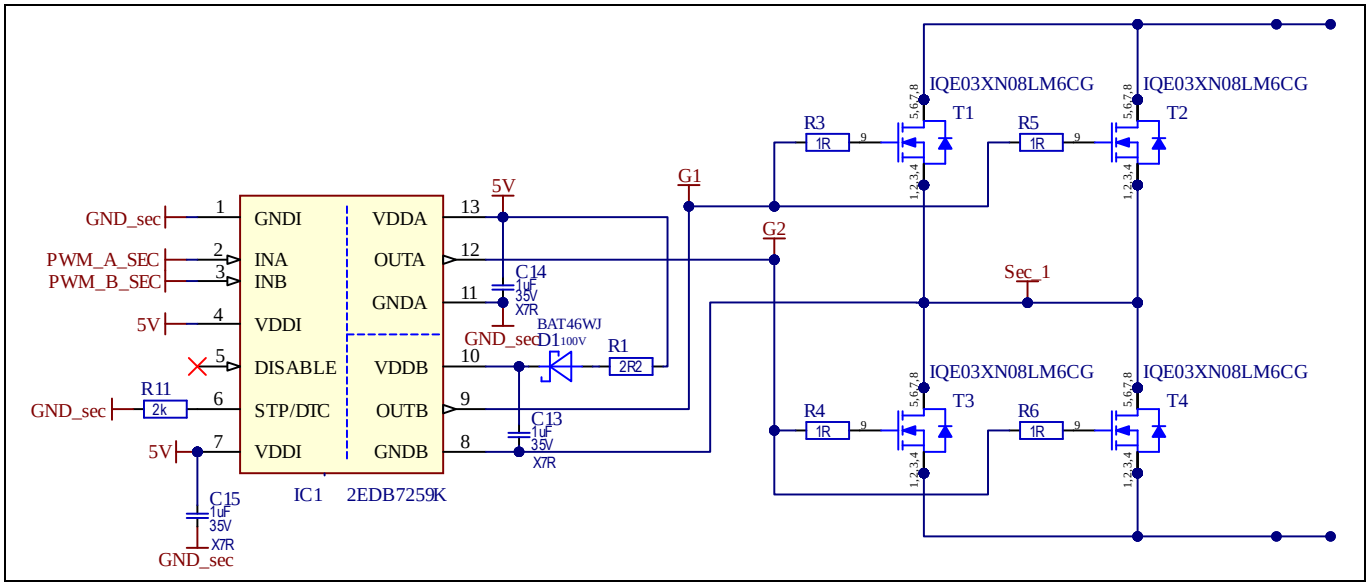


Figure 42 Driving OptiMOS™ on the secondary side of the LLC converter

3.3 Hold-up time extension, in-rush, and re-rush current control

Besides integrating the LLC magnetics to achieve 100 W/in^3 power density, another viable and widely accepted approach is to implement a reduction of the bulk capacitance. If, under steady-state conditions, the converter can operate with a lower bulk capacitance, satisfying the following criteria, the hold-up extension can be handled with additional circuit which allows for a lower bulk voltage during a line cycle dropout (LCDO) event:

- Bulk voltage not exceeding the electrolytic capacitors' maximum voltage rating, as well as the current stress in the capacitors within their ratings
- The energy stored in the bulk capacitors is enough to power the LLC converter for 20 ms at full output power (8.0 kW) during an LCDO event
- Maximum AC input peak voltage above the minimum bulk voltage to ensure proper PFC operation, i.e., keeping the power factor and total harmonic distortion within limits

A similar baby-boost implementation has been used in [6] with minor modifications. In the case of REF_8KW_HFHD_PSU, to save layout room, the electromechanical relay has been replaced with a static switch in series with the electrolytic capacitors. Moreover, because of the higher bulk capacitance compared to REF_3K3W_HFHD_PSU, a high current condition through the electrolytic capacitor can be triggered after an LCDO event. For this reason, a re-rush switch has been implemented in parallel to a 1.5 Ω resistor to limit possible peak currents after every LCDO event.

Figure 43 shows an excerpt of the M100001428 schematic which includes the baby-boost converter, the in-rush, and the re-rush switches implemented in REF_8KW_HFHD_PSU. With reference to the schematic, V_{TP} is the totem pole DC-link voltage, V_{bulk} is the bulk voltage, and V_+ is the input of the LLC converter. When an LCDO event occurs and the PFC controller detects no AC input voltage together with a bulk voltage V_{bulk} below 390 V, the baby-boost circuit is activated. At this point, the static switch (reference designators Q1 and Q2 in M100001428) disconnects the V_+ rail from the V_{bulk} rail and the baby-boost starts operating. Since the V_{bulk} rail is not the input voltage of the LLC converter at this point, a lower voltage is allowed on the bulk capacitor bank (reference designators C15-C21 in M100001428) to extract the 160 J required during the 20 ms hold-up at 100% of output power.

The baby-boost circuit operates at a switching frequency of 190 kHz, and it is disabled if one of the following conditions is triggered:

- **If the grid voltage is lost for >20 ms**: Timing limitation is applied to the baby boost to stop the PSU from delivering power to the load if the AC voltage is lost for more than 20 ms [1]. As an additional safety measure to limit the possible re-rush current, the baby-boost operation is also stopped if the measured V_{bulk} voltage is lower than the minimum threshold of 180 V as well. However, this condition is not normally triggered if the capacitance of the bulk capacitors bank is correct and within the specified tolerances
- **If the grid voltage is lost for ≤20 ms**: Under this condition the AC input voltage recovers before the 20 ms limit and the PFC starts recharging the electrolytic caps. The static switch is kept open, and the baby-boost operates until V_{bulk} is fully charged, and (V_{bulk} - V_+) <10 V

Additionally, in case the grid voltage is lost for ≤20 ms, V_{bulk} happens to be lower than the AC voltage, therefore a control of the re-rush current is needed. For this reason, the re-rush switch (reference designator Q3 and Q6 in M100001428) is driven such that the current peaks flow through the resistor R3, which limits the peak re-rush current.

Figure 44 shows an example of an LCDO event when the grid voltage is lost for <20 ms (case b), so that the PFC restarts and recharges the electrolytic capacitors bank.

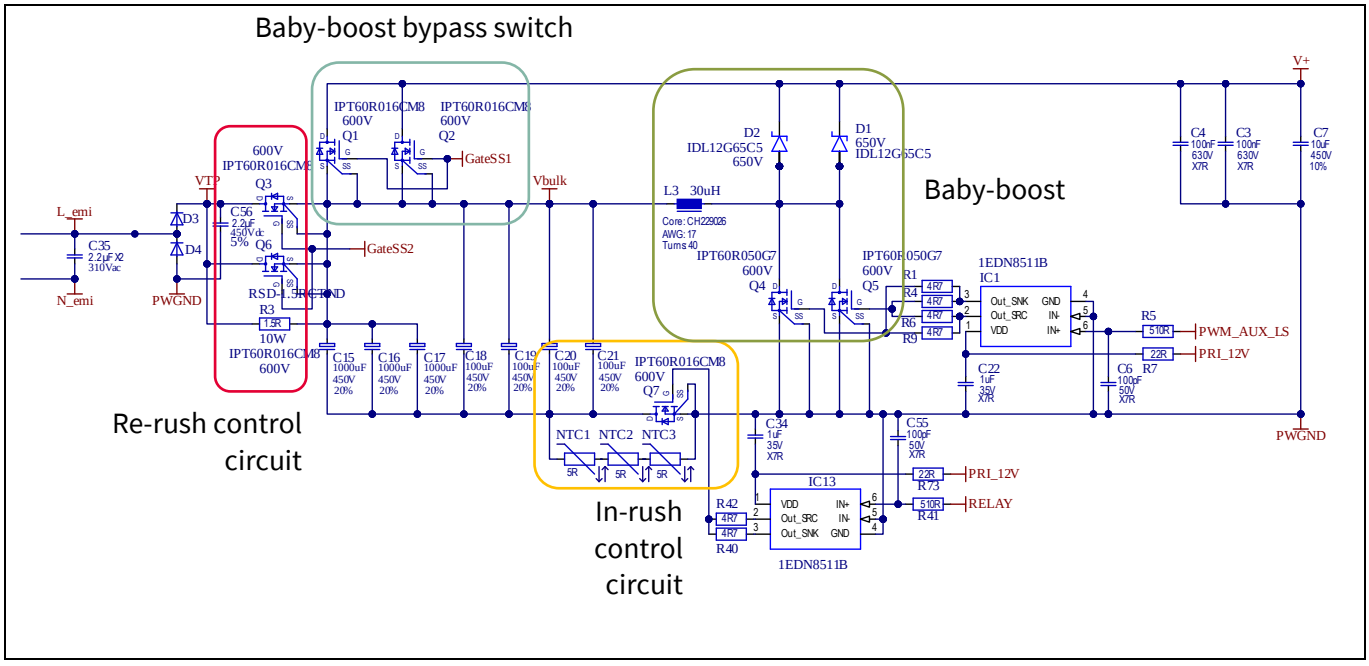


Figure 43 Schematic of the baby-boost circuity on the main board to comply with LCDO requirement

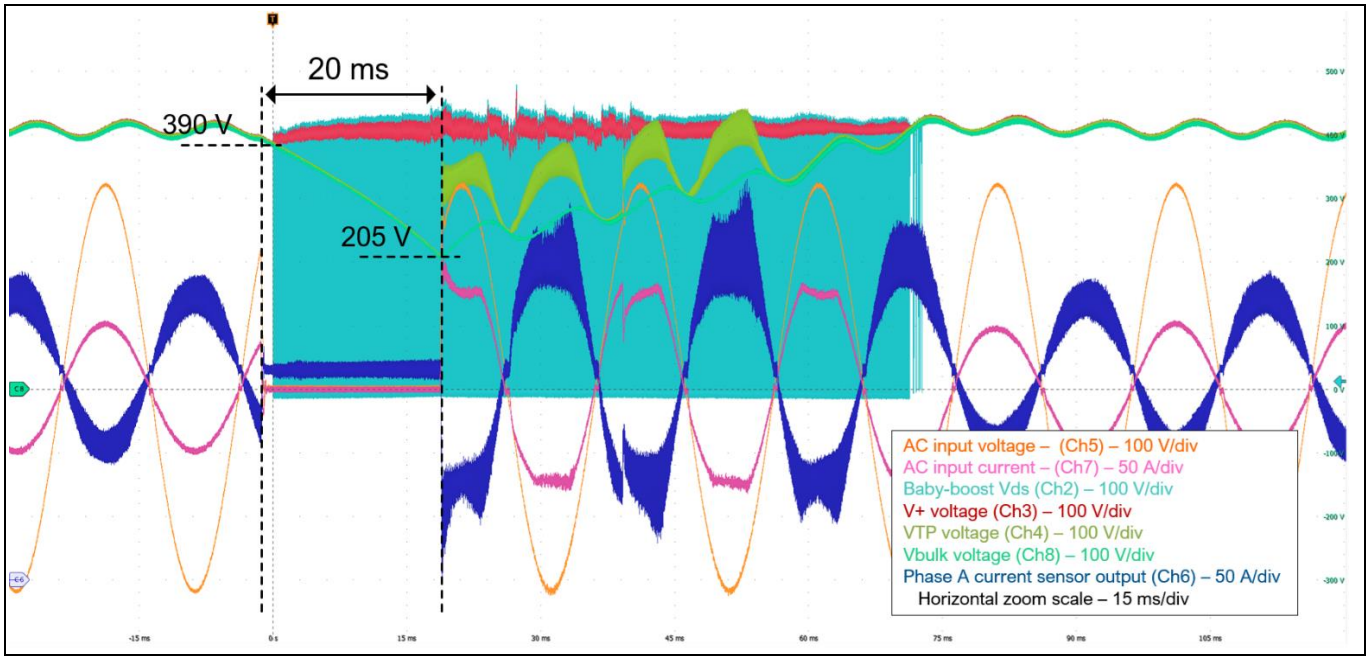


Figure 44 Baby-boost operation during LCDO event at 100% load

4 Experimental results

4.1 Steady-state performance

4.1.1 PSU efficiency and power losses

Figure 45 recalls the efficiency measurements for steady-state operation of the full PSU at different AC voltages already presented in Section 2.6. The efficiency measurements have been obtained with a WT5000 power analyzer with 10 kHz input and output line filters, including fan power consumption.

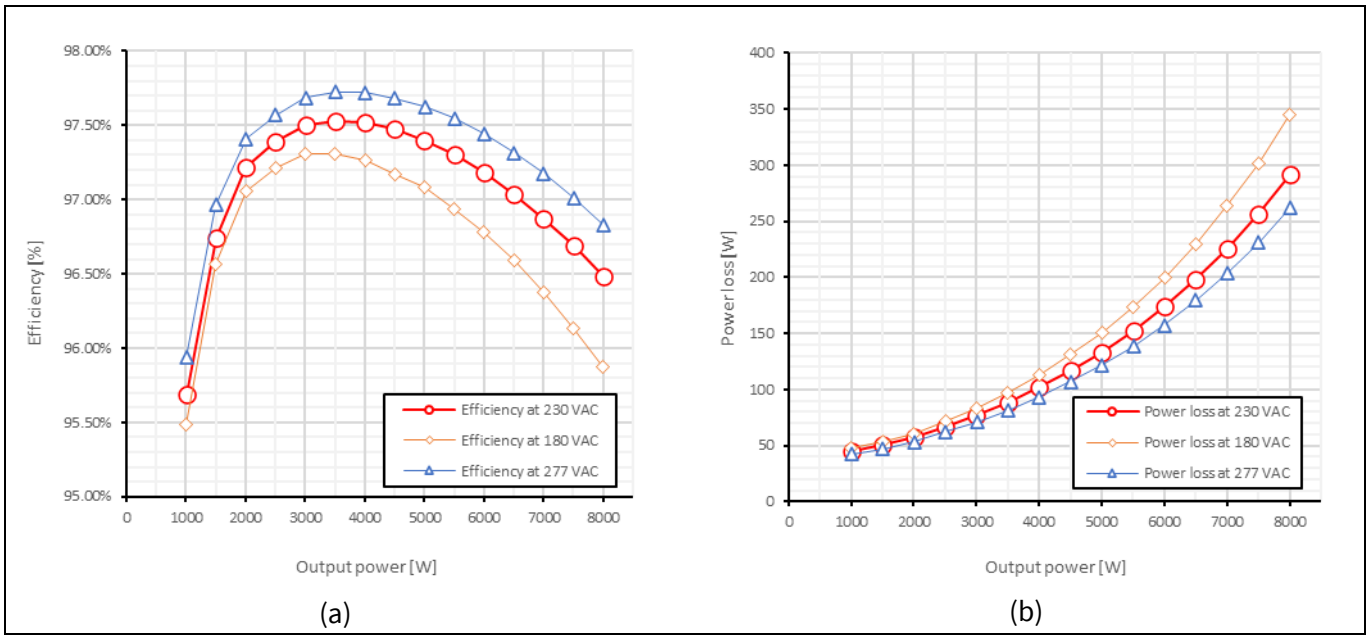


Figure 45 Measured efficiency (a) and power losses (b) of REF_8KW_HFHD_PSU for different input line voltages (180 V_{AC}, 230 V_{AC}, and 277 V_{AC}), fan power consumption included

4.1.2 PSU power factor correction and iTHD

Figure 46 and Figure 47 show the power factor and the total input current harmonic distortion (iTHD) measured at 230 V_{AC} and 180 V_{AC} line voltages, 50 Hz. The iTHD and PF measurements have been performed on the full PSU operating in steady state conditions.

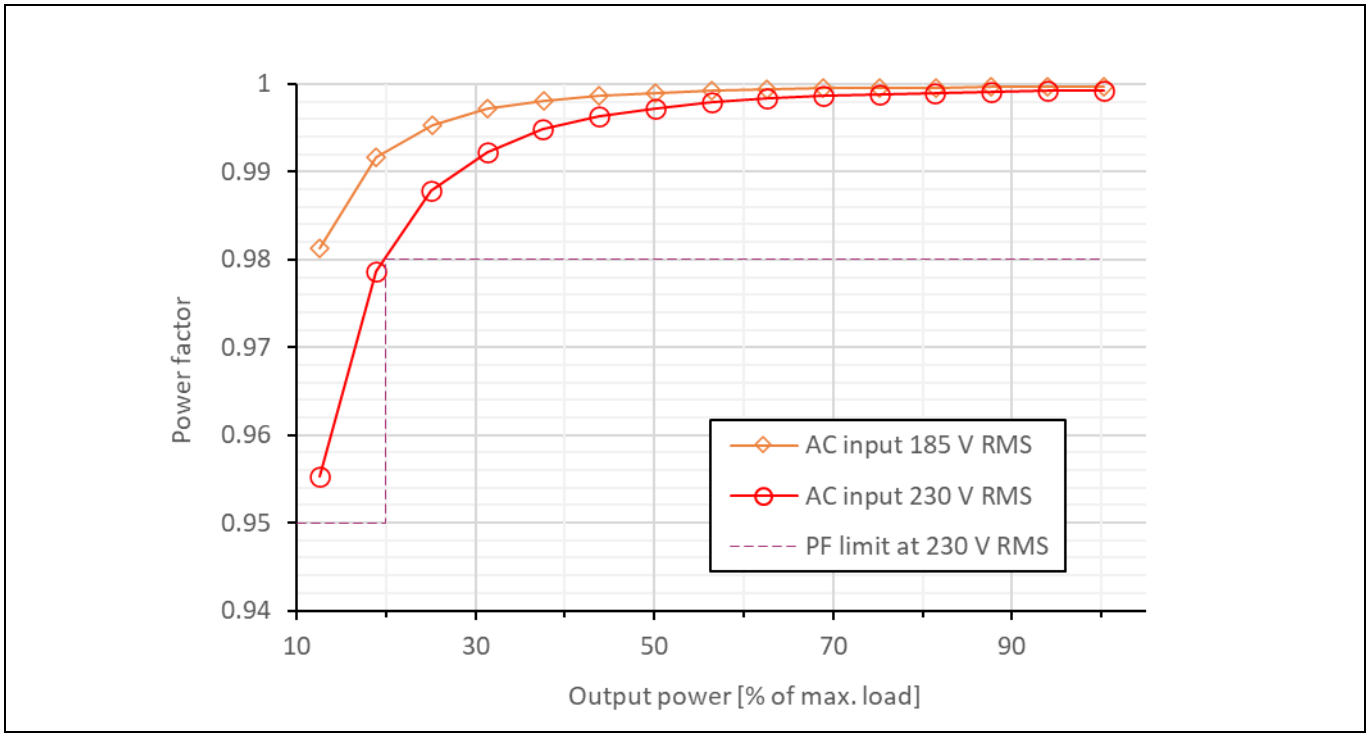


Figure 46 Power factor (PF) of the PSU and OCP power factor limit

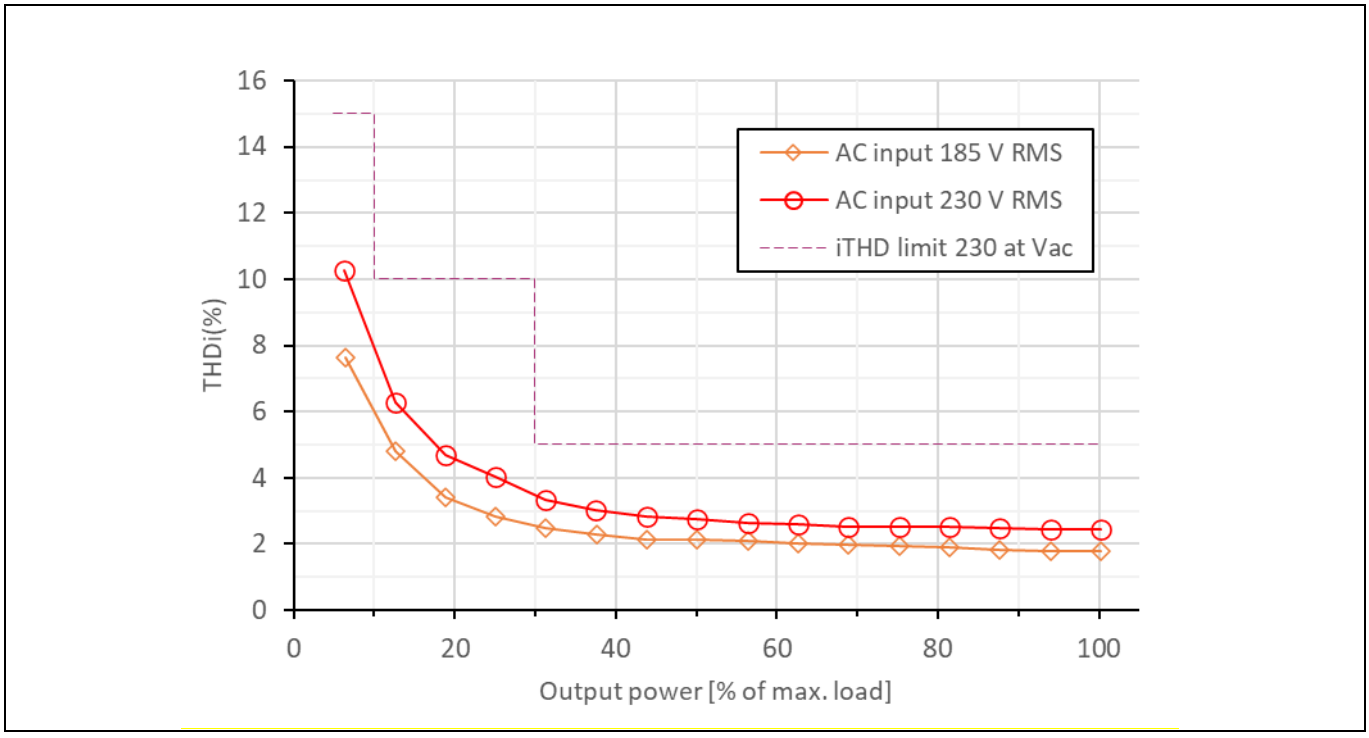


Figure 47 Input current total harmonic distortion (iTHD) of the PSU and OCP iTHD limit

4.1.3 PSU startup

Complete PSU startup is achieved within 1.2 s after the AC grid voltage is applied to the unit. After the AC input voltage is applied, the PFC starts boosting the bulk voltage until the 405 V average reference is achieved. Eventually, the LLC starts supplying power to the load. A full PSU startup sequence is presented in Figure 48.

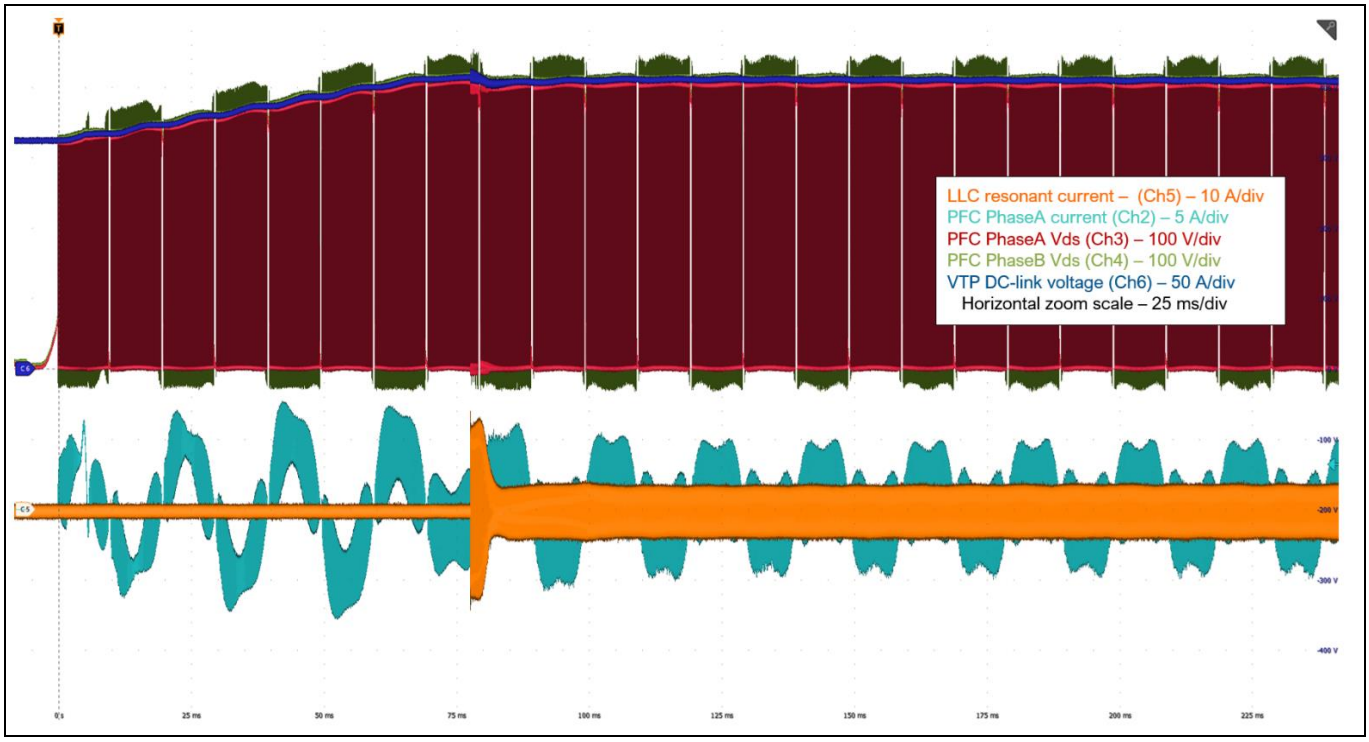


Figure 48 PSU startup at 230 V_{AC} input, full load

Startup of the LLC converter is shown in detail in Figure 49. The startup starts with 15 open loop pulses, with the first one asymmetric and shorter (1/4 T_{SW}) to reduce peak current. Switching frequency during startup is 2.5 MHz, and the total startup time takes around 4 ms until the output is within ±10% of the final value.

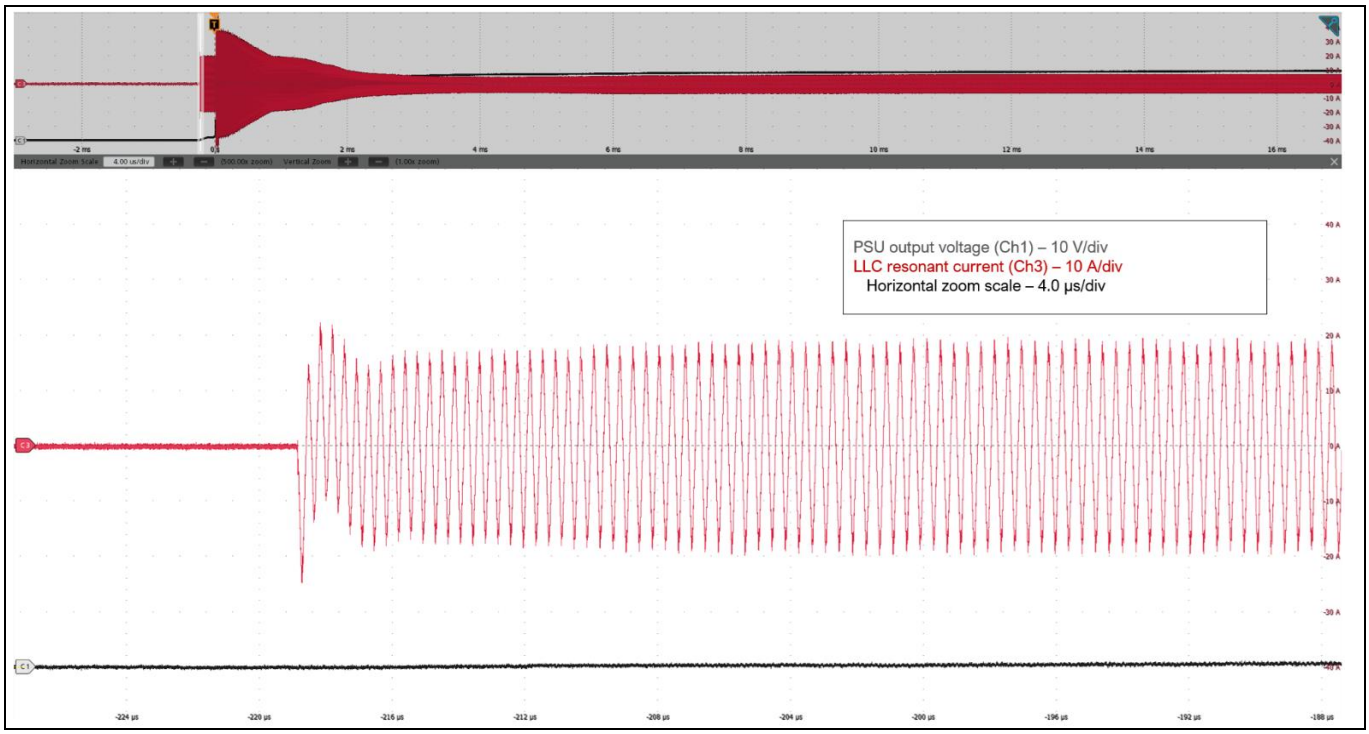


Figure 49 LLC converter startup

4.1.4 Output and bulk voltage ripple

Figure 50 shows the PSU waveforms during steady state operation at 230 V_{AC} input, full load. VTP voltage (equal to V_{bulk} in steady state), 50 V_{DC} LLC output voltage, PFC stage A, and LLC resonant currents are shown.

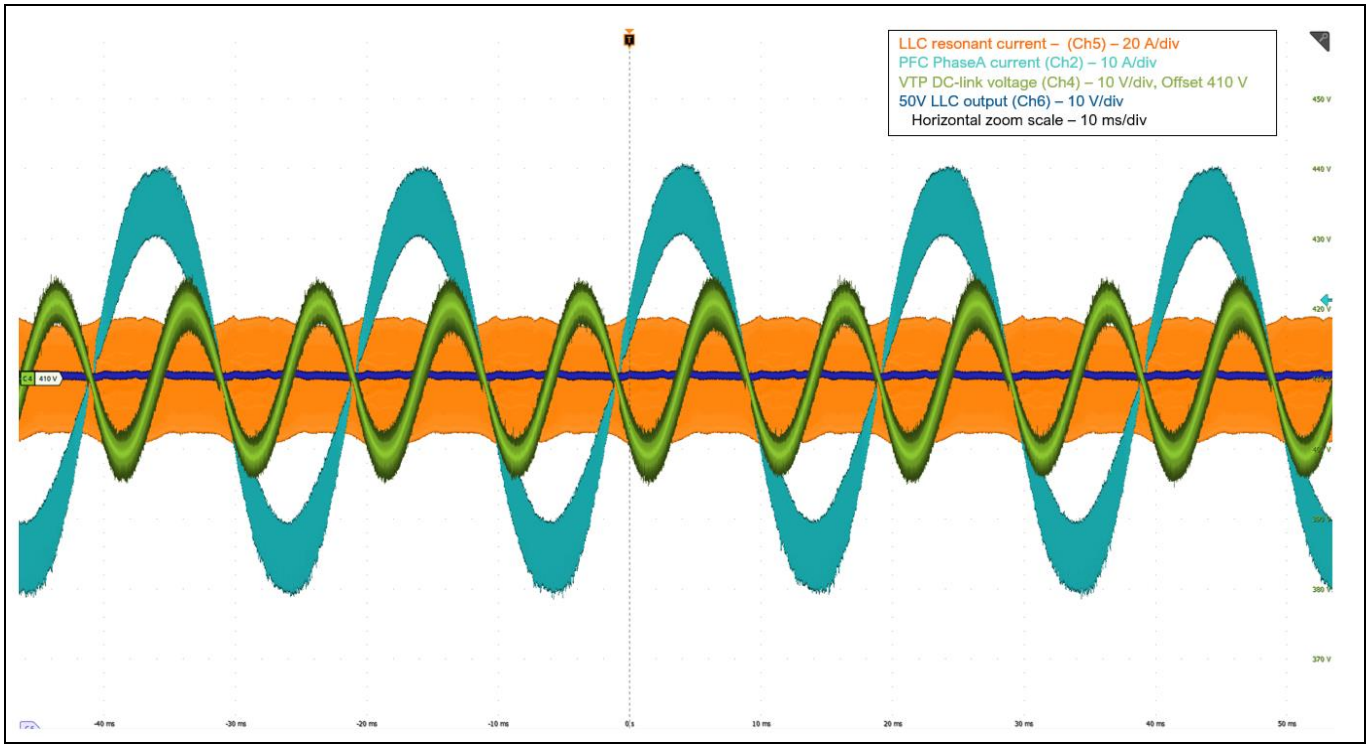


Figure 50 LLC resonant and PFC currents, and output and bulk voltages at 100% load, 230 V_{AC}

During steady state operation at 230 V_{AC} input, the nominal bulk voltage has been selected to be 405 V and has a double line frequency ripple of around 23 V (see Figure 51 (a)). When operating at a higher AC input voltage compared to nominal (i.e. from 230 V_{AC} to 277 V_{AC}), the bulk voltage is increased to keep the power factor correction operational. In particular, the measured AC voltage is compared to 240 V_{AC} and 255 V_{AC} RMS thresholds, and the bulk voltage is increased consequently. Figure 51 (b) shows the bulk voltage at 277 V_{AC} input voltage – nominal bulk voltage is 411 V, with a double-line frequency ripple of around 23 V peak-to-peak.

Operation at 305 V_{AC} on the PSU could be addressed by increasing the bulk voltage in steady state operation, and slightly changing the turn ratio of the LLC transformer. This could allow operation at higher voltages while keeping the LLC under the same optimal operating conditions.

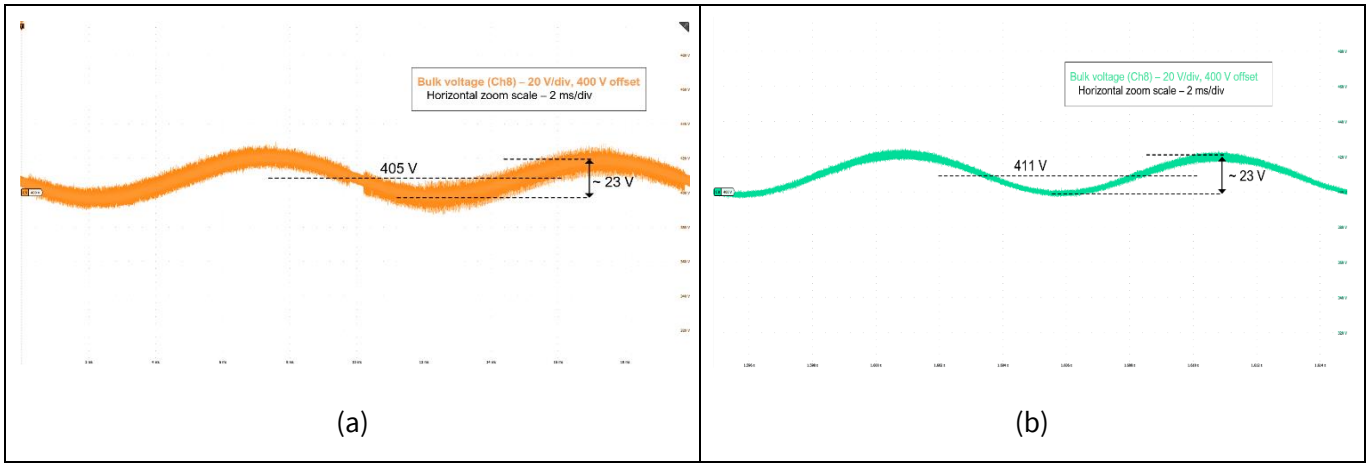


Figure 51 Bulk voltage ripple at 100% load, 230 V_{AC} (a) and 277 V_{AC} input voltage (b)

Figure 51 shows the PSU output voltage ripple, together with the AC input voltage and current. The voltage at the output is measured by means of a passive probe with a 100 MHz bandwidth. A 0.1 µF multilayer ceramic capacitor for the measurement has been used [1], and is already placed on the adapter board PW300001428. The measurement shows an output ripple of 160 mV peak-to-peak, within the 500 mV peak-to-peak voltage limit as per specification.

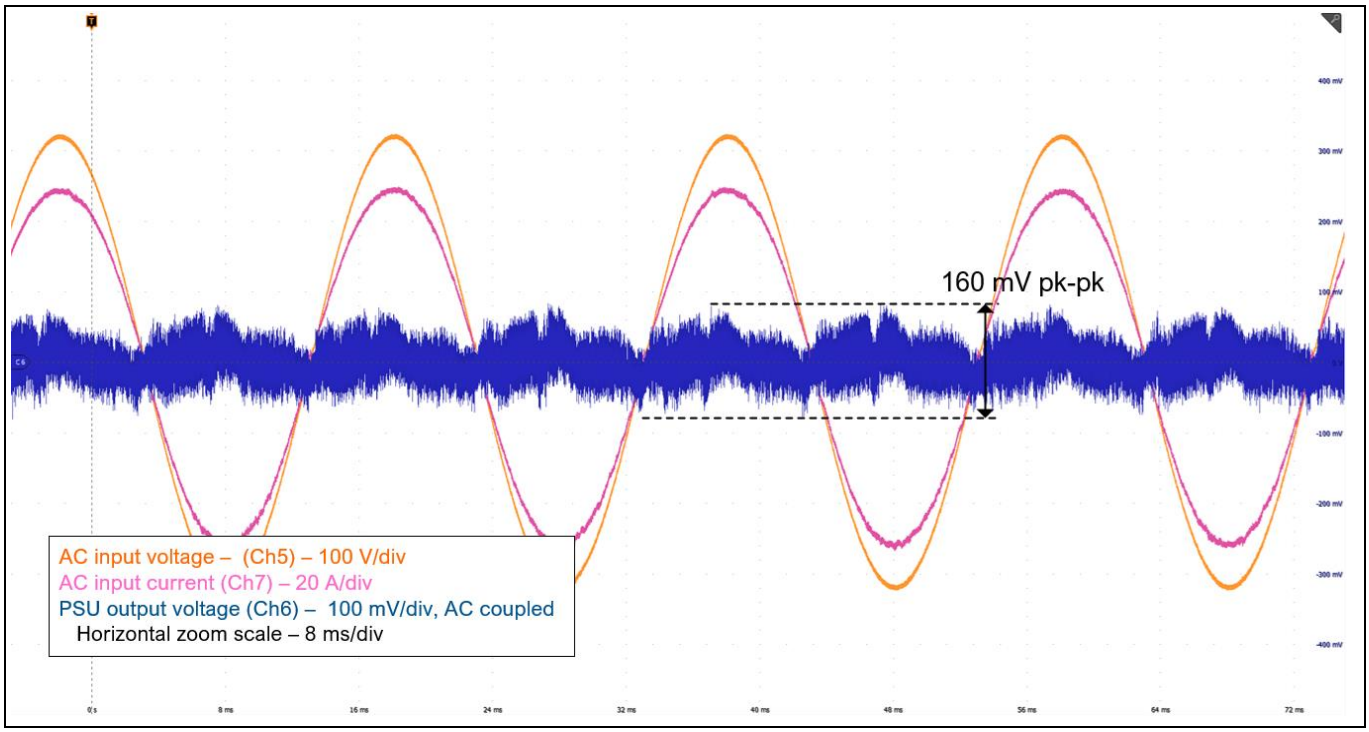


Figure 52 PSU output voltage ripple at 100% load

4.1.5 Bridgeless interleaved totem-pole PFC

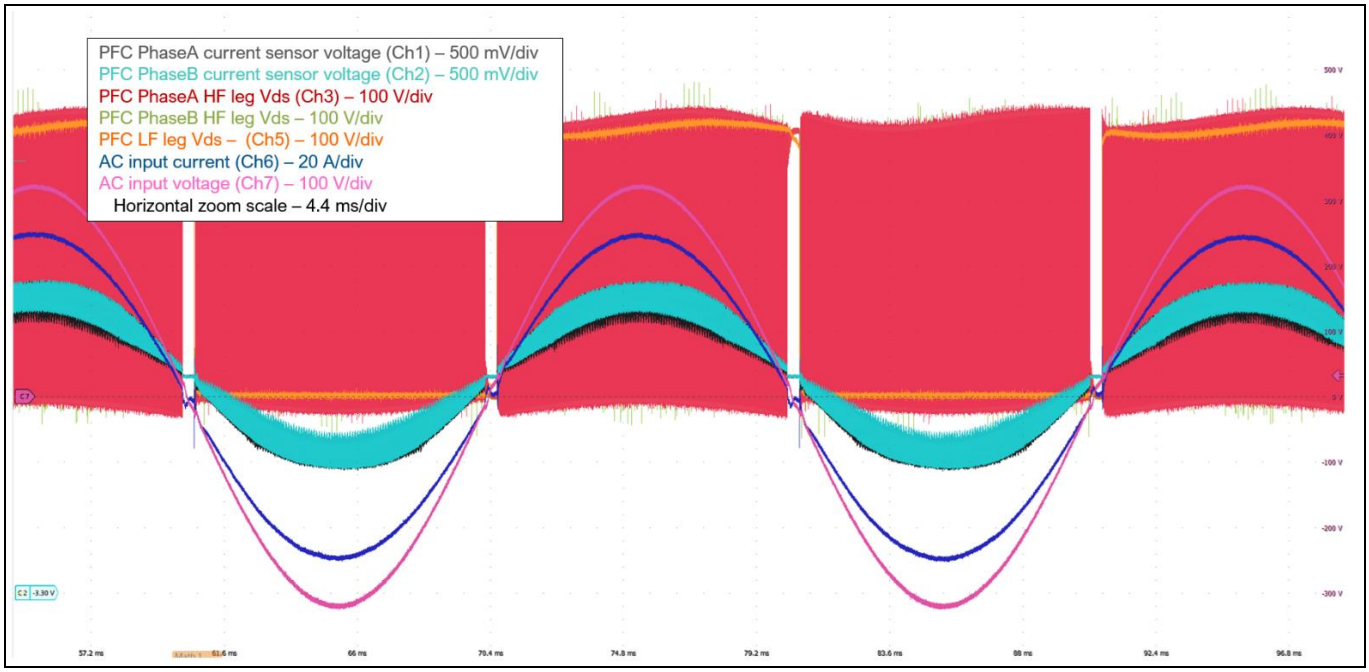


Figure 53 PFC steady-state operation at 230 V_{AC}, full load

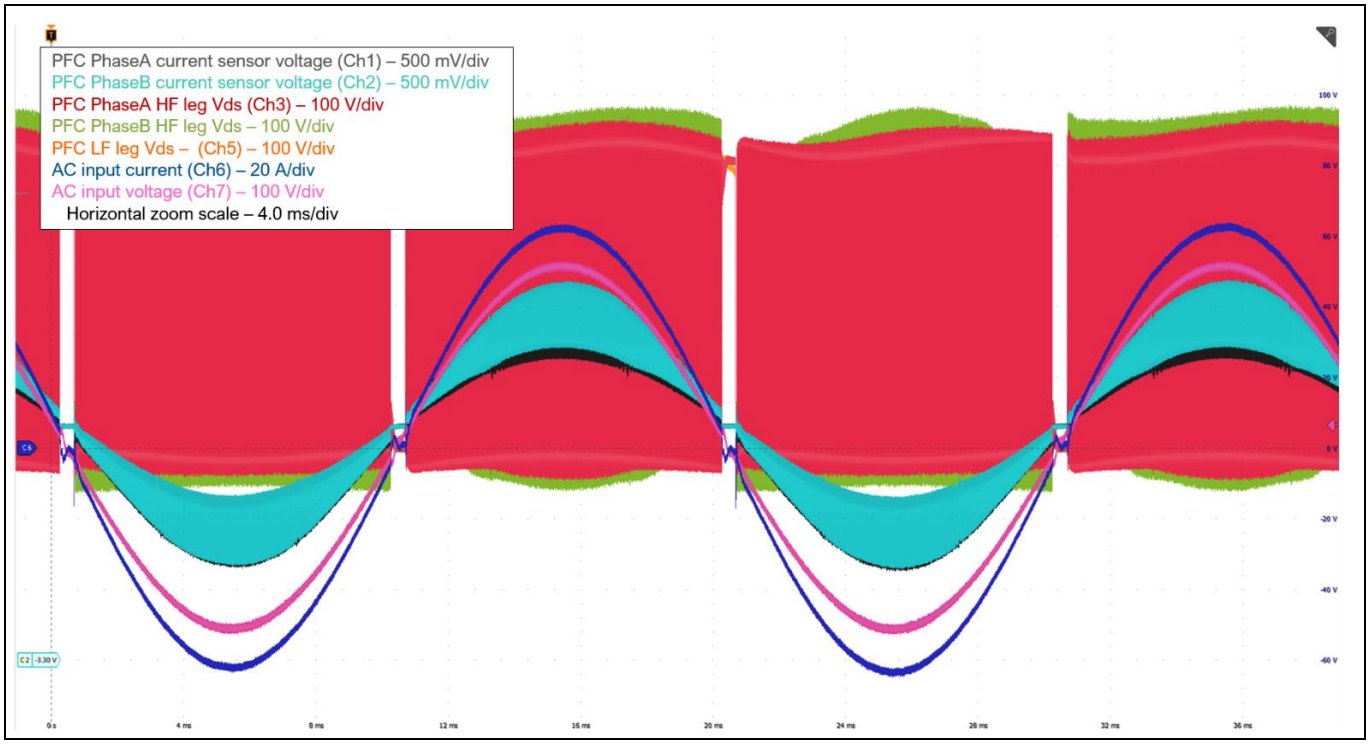


Figure 54 PFC steady-state operation at 180 V_{AC}, full load

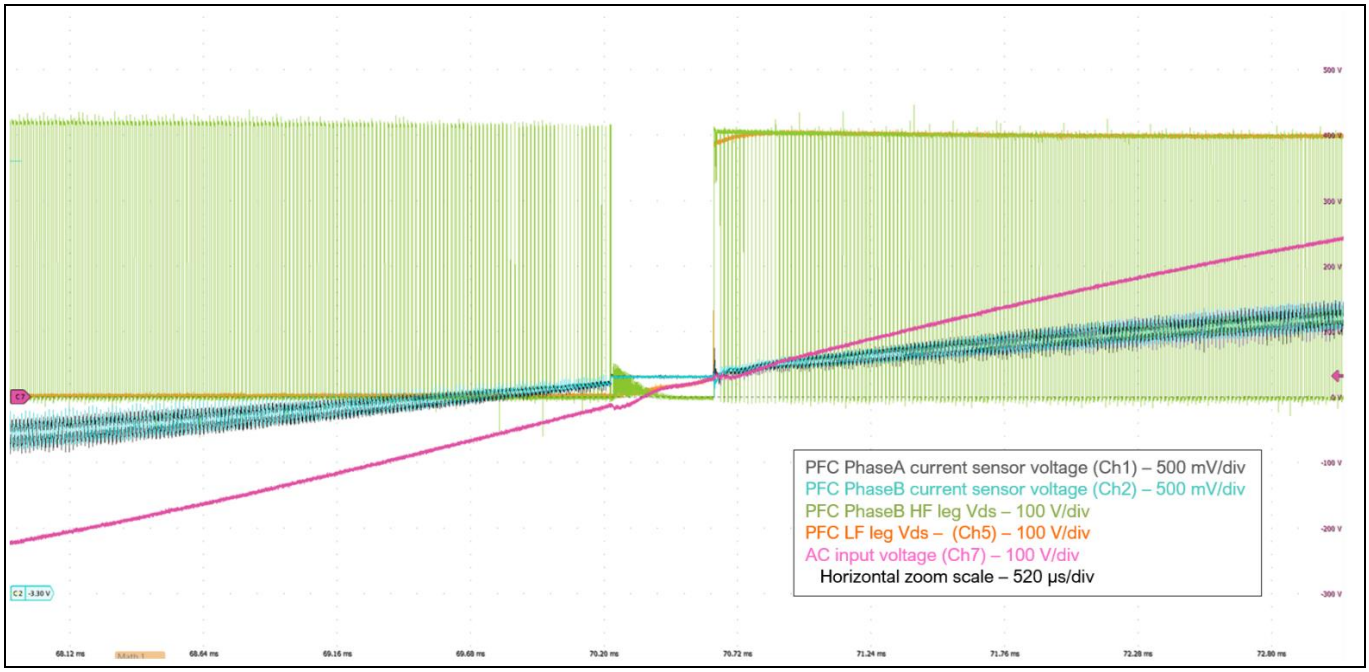


Figure 55 PFC zero crossing A

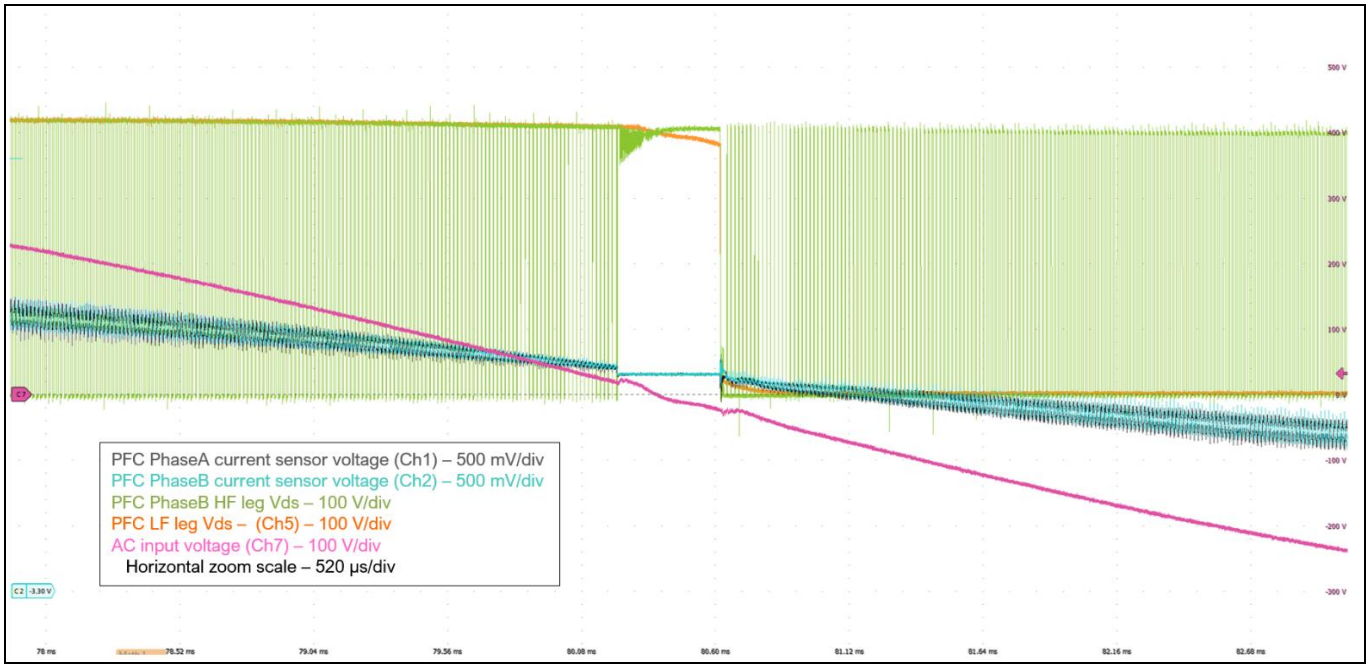


Figure 56 PFC zero crossing B

4.1.6 Full-bridge to full-bridge LLC converter

The FB/FB LLC converter uses CoolGaN™ IGT65R035D2 on the primary side and IQE033N08LM6CG for the secondary synchronous rectification stage. Figure 57 and Figure 58 show the secondary XFMR voltage, the resonant current, and the bulk voltage during PSU operation at full load. The maximum and the minimum frequency of the LLC are also shown.

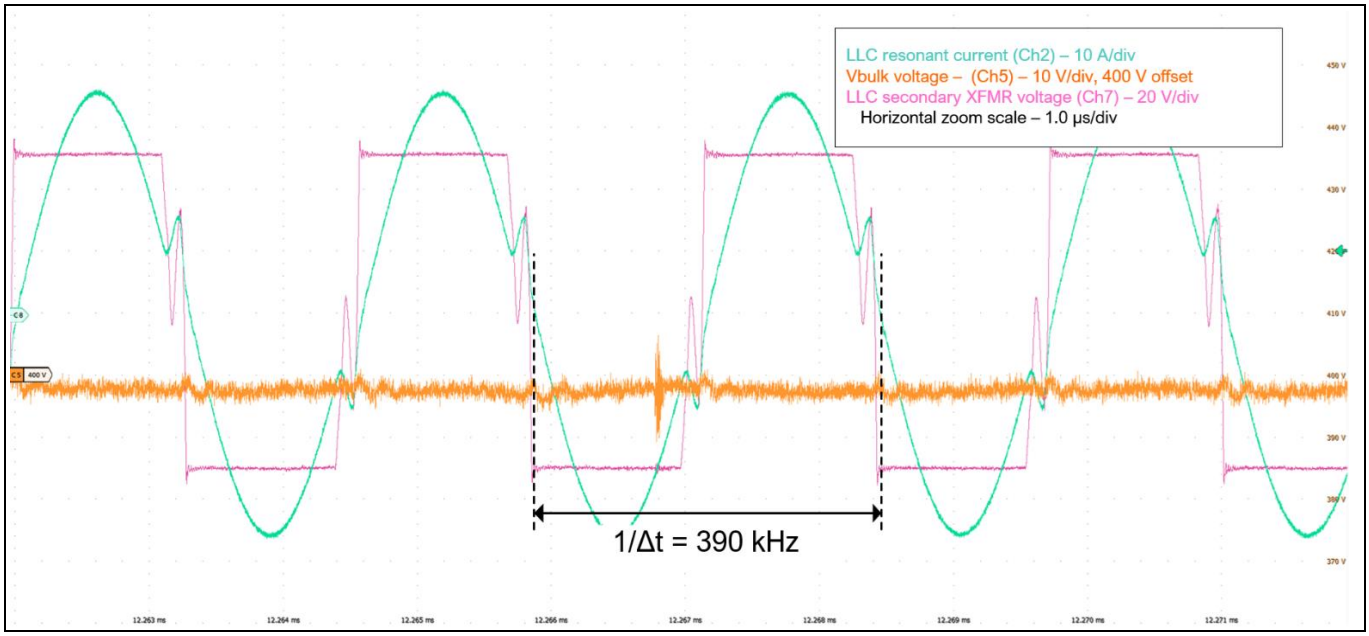


Figure 57 **LLC waveforms during steady-state operation, full load, 230 V_{AC} input, V_{bulk} at minimum peak of the double line frequency ripple (395 V)**

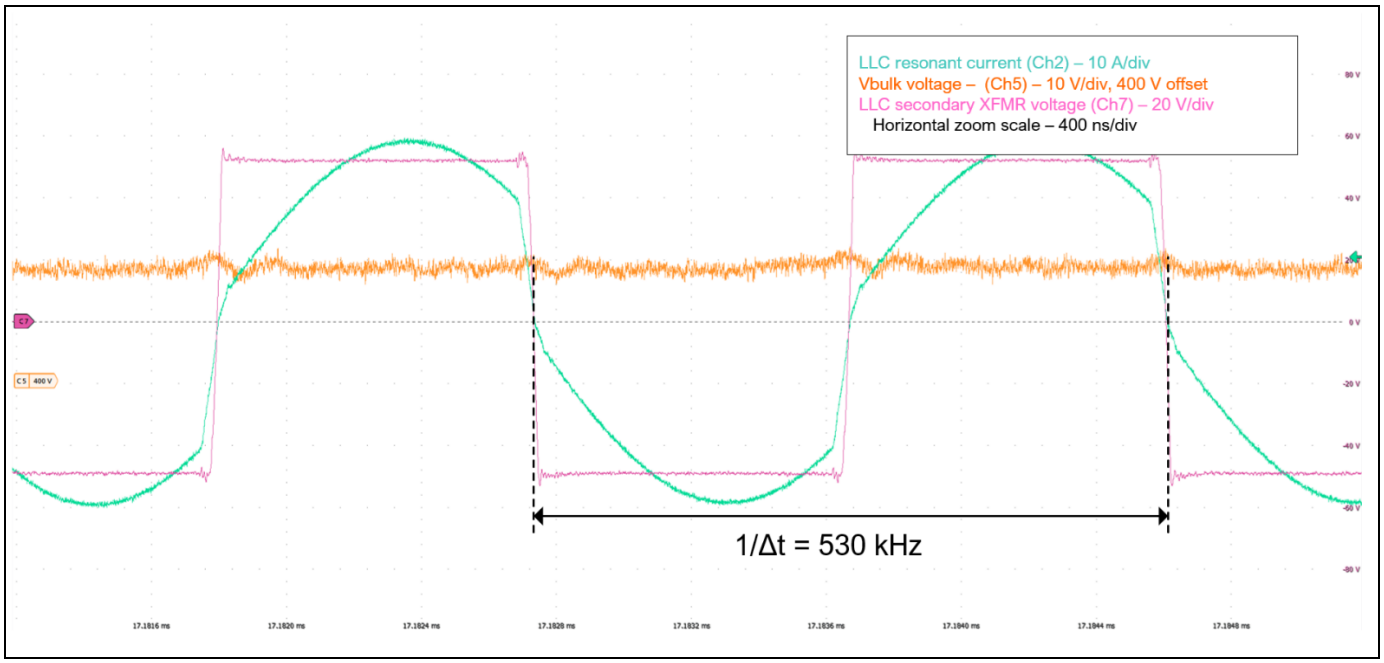


Figure 58 **LLC waveforms during steady-state operation, full load, 230 V_{AC} input, V_{bulk} at maximum peak of the double line frequency ripple (420 V)**

4.1.7 Thermal performance

Thermal performance of the full PSU has been simulated and verified under several PSU operating conditions. Figure 59 indicates airflow direction and path in the unit, while Figure 60 and Figure 61 show the preliminary results of thermal simulations executed on an early prototype of the unit. Table 5 reports the hotspot temperatures in some relevant operating conditions and measured temperatures at the thermal stability point. The measured results provide enough margin to operate at maximum ambient temperature of 45°C.

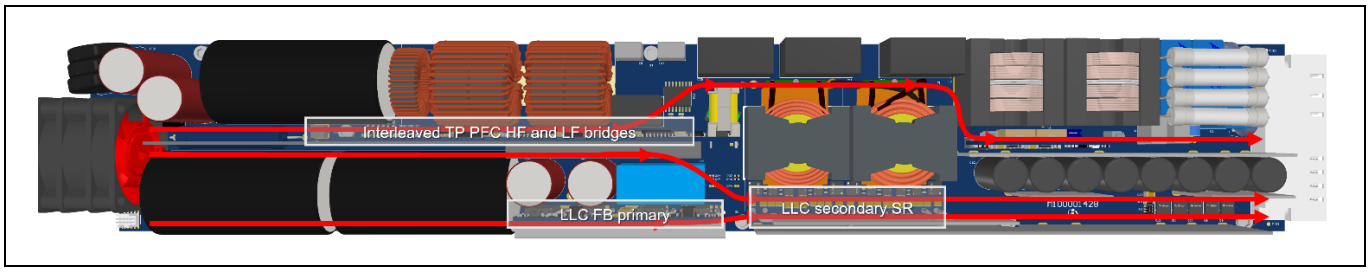


Figure 59 PSU airflow direction

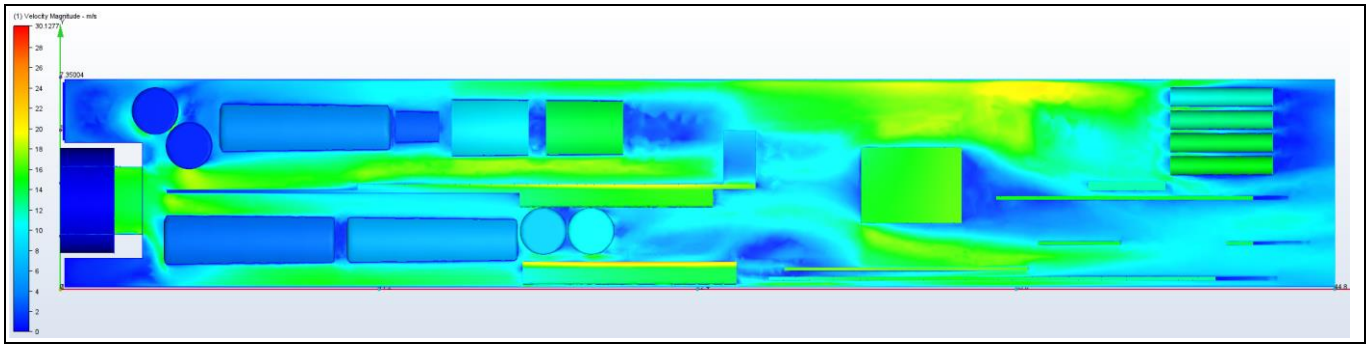


Figure 60 Airflow velocity magnitude - cross section close to PSU ceiling

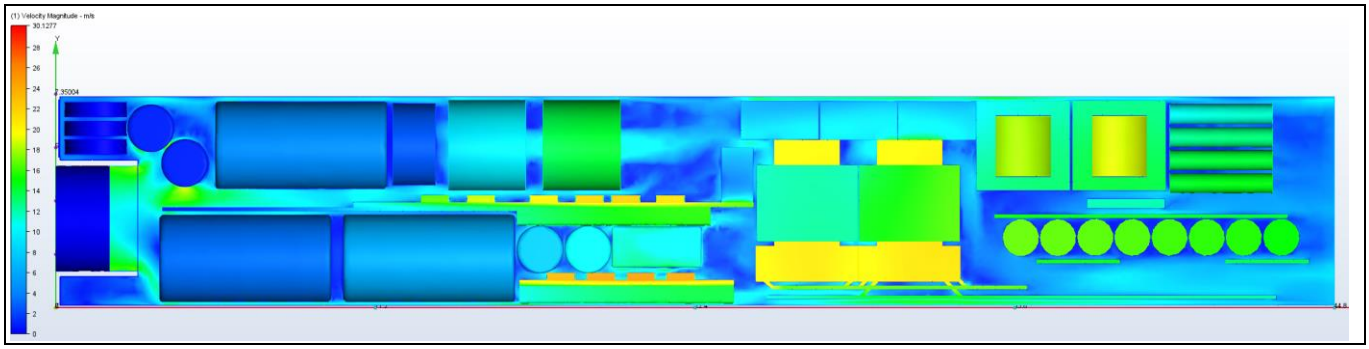


Figure 61 Airflow velocity magnitude - cross section at PSU center

Table 5 PSU hotspot temperatures

Condition[7]	XFMR-B SR MOSFETs	XFMR-A SR MOSFETs	PFC HF bridge MOSFETs	LLC FB MOSFETs
100% of rated output power AC input voltage: 180 V	103°C	89°C	80°C	67°C
100% of rated output power AC input voltage: 230 V	100°C	87°C	63°C	64°C
50% of rated output power AC input voltage: 230 V	90°C	78°C	58°C	60°C

[7] All temperatures are measured with J-type thermocouples, PSU inside chassis, 25°C ambient temperature and at thermal stability

4.2 Dynamic performance

4.2.1 Output load transients

REF_8KW_HFHD_PSU has been tested for load transients, from 10-50% and from 10-90% (and vice versa), with a 1 A/µs slew rate and a 10 Hz repetition rate as shown in Figure 62. PSU ruggedness against zero to full load transient and vice versa have been also tested. Feed-forward of the PSU output current to the PFC control loop has been implemented to optimize the dynamic performance, as discussed in Section 3.1.4.

Figure 63 and Figure 64 show a detailed view of the 10-90/90-10% and 10-50/50-10% load transients respectively. During 10-50/50-10% transients, a maximum V_{OUT} overshoot/undershoot of 380 mV peak has been observed (within the 500 mV limit [1]), while during 10-90/90-10% transients it turned out to be 560 mV peak (within the 1.0 V limit [1]).

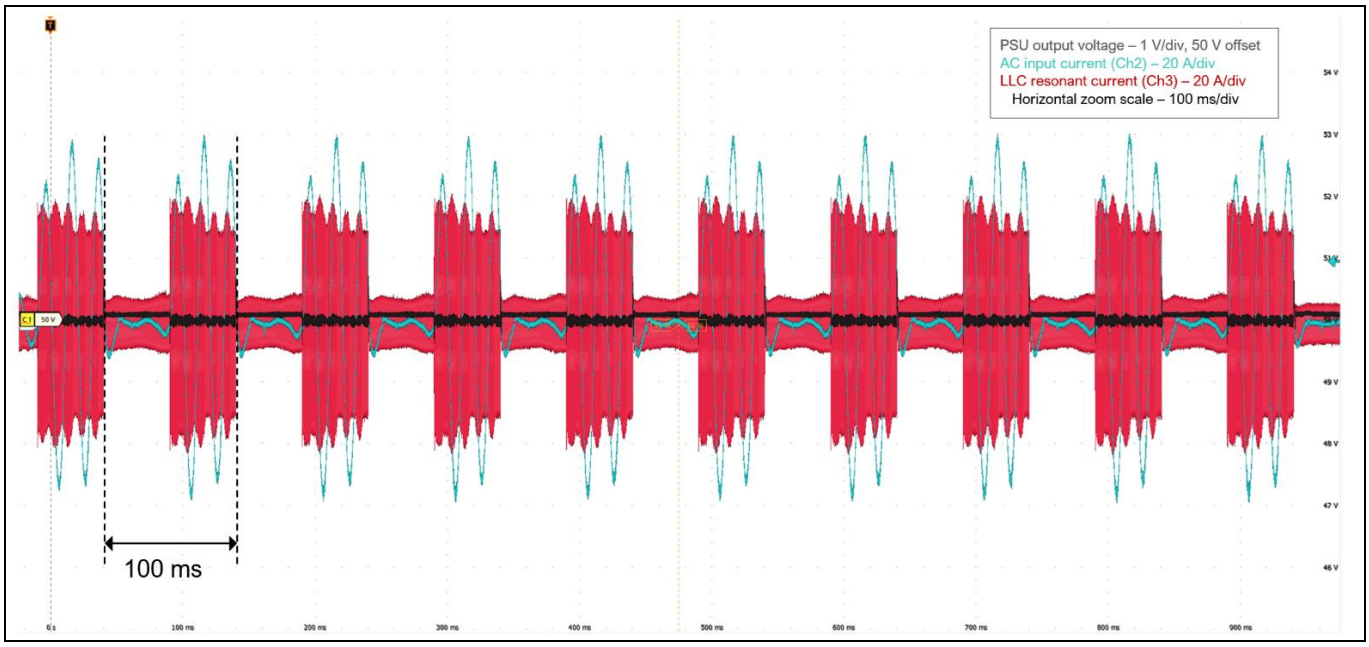


Figure 62 PSU repetitive load transient, 10-100% and 100-10% output load

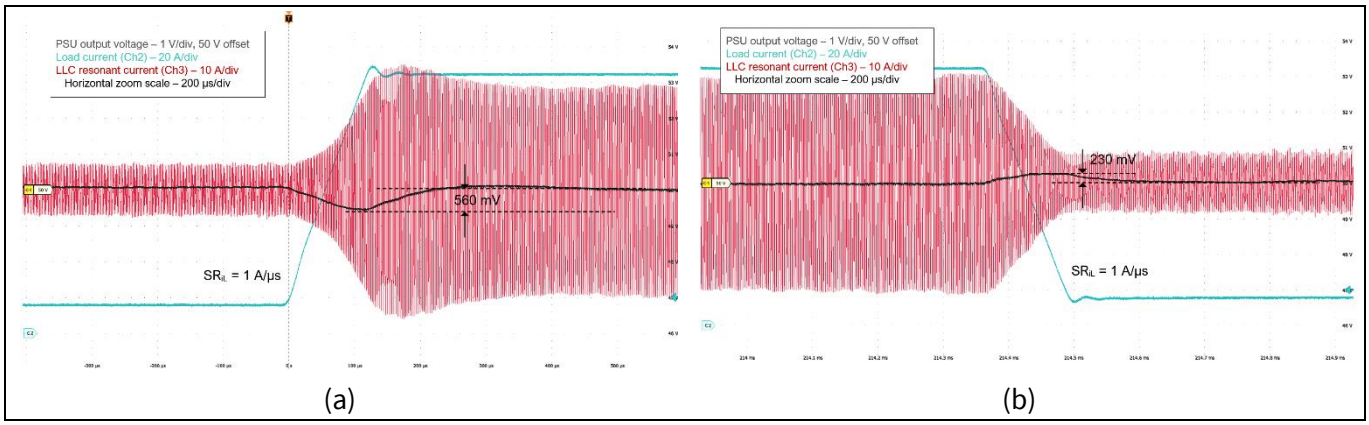


Figure 63 PSU load transient at 10-90% (a) and 90-10% (b) output load, detailed view

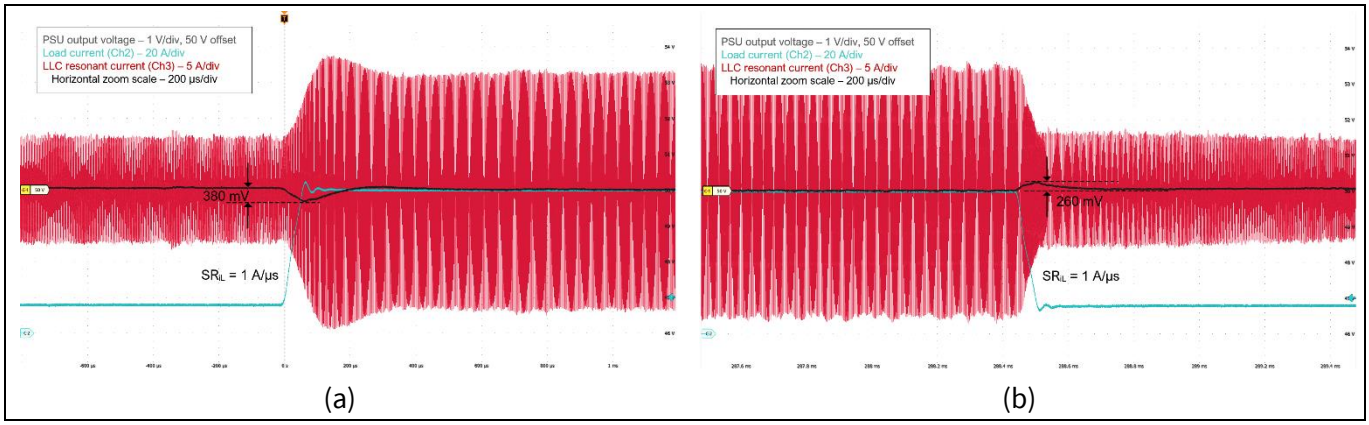


Figure 64 PSU load transient at 10-50% (a) and 50-10% (b) output load, detailed view

4.2.2 AC input voltage sag

REF_8KW_HFHD_PSU has been tested for AC line transients of 230 V/180 V RMS and 230 V/160 V RMS for a time duration of 500 ms. Figure 65 and Figure 66 report the relevant waveforms for the two testing conditions.

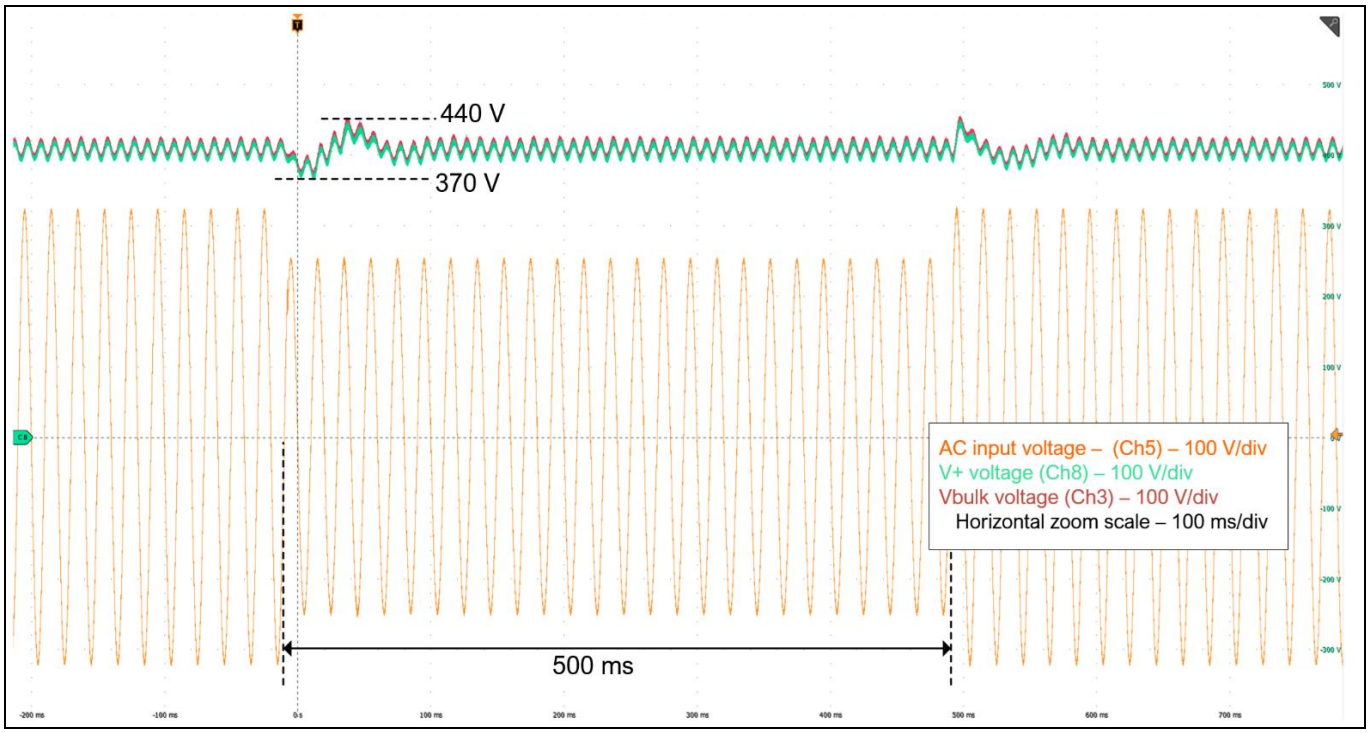


Figure 65 AC input voltage sag, 230 V_{AC} to 180 V_{AC}, 100% output load

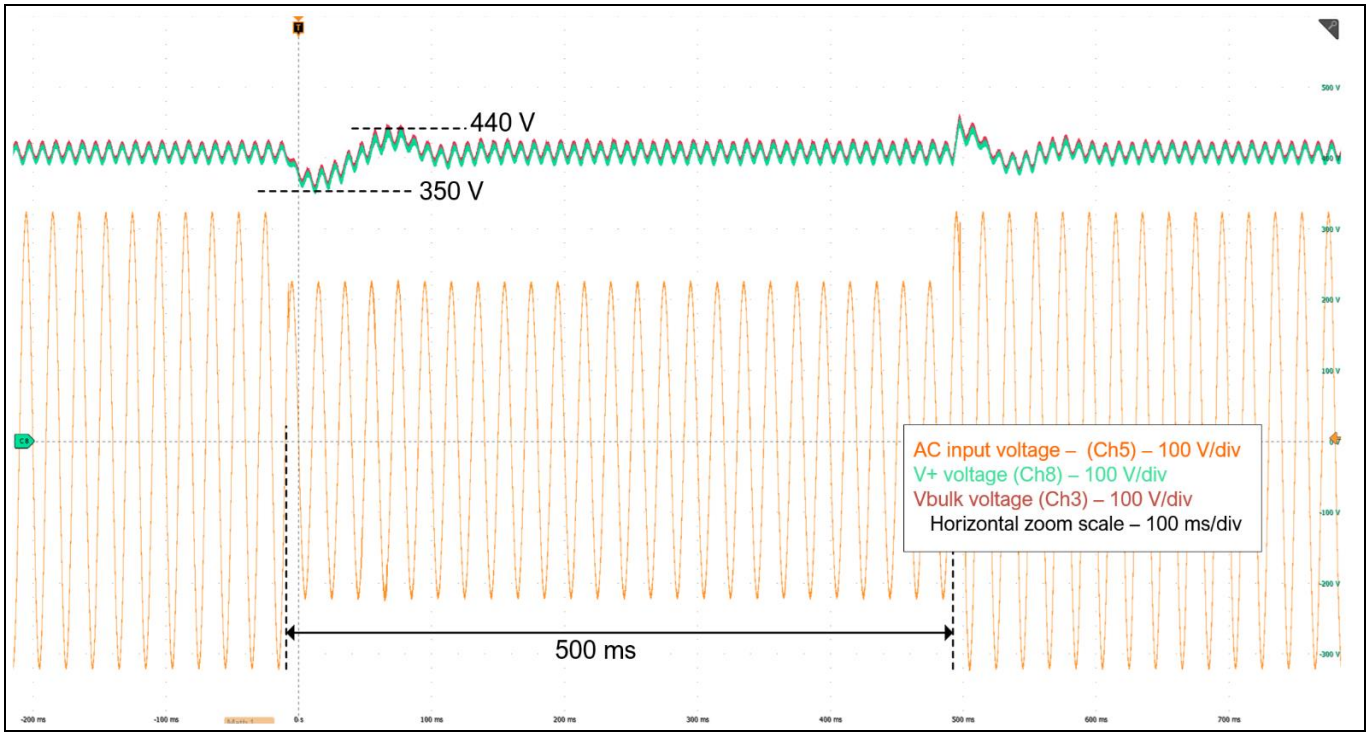


Figure 66 AC input voltage sag, 230 V_{AC} to 160 V_{AC}, 100% output load

4.2.3 Hold-up time extension and re-rush current limit circuits

REF_8KW_HFHD_PSU implements a baby-boost circuit to meet 20 ms hold-up time requirements. Its operating principle is discussed in Section 3.3. Hold-up time extension with the baby-boost converter has been validated on the PSU.

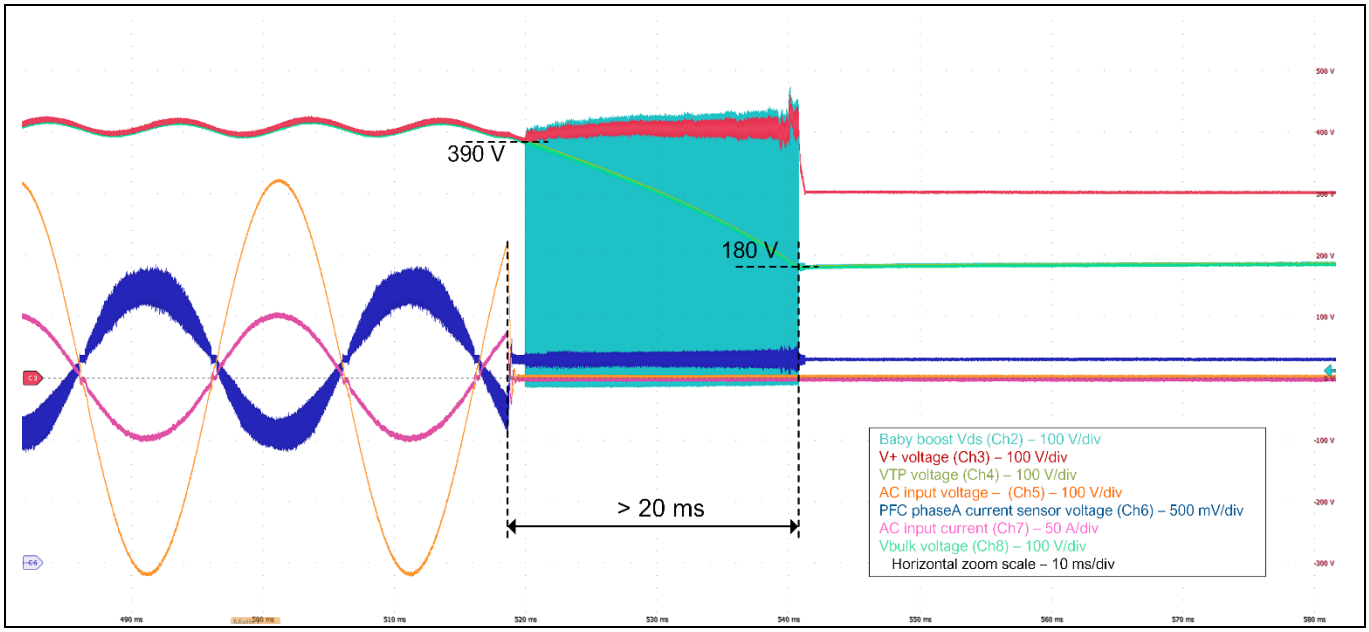


Figure 67 Hold-up time at 100% of the rated load with LCDO duration >20 ms

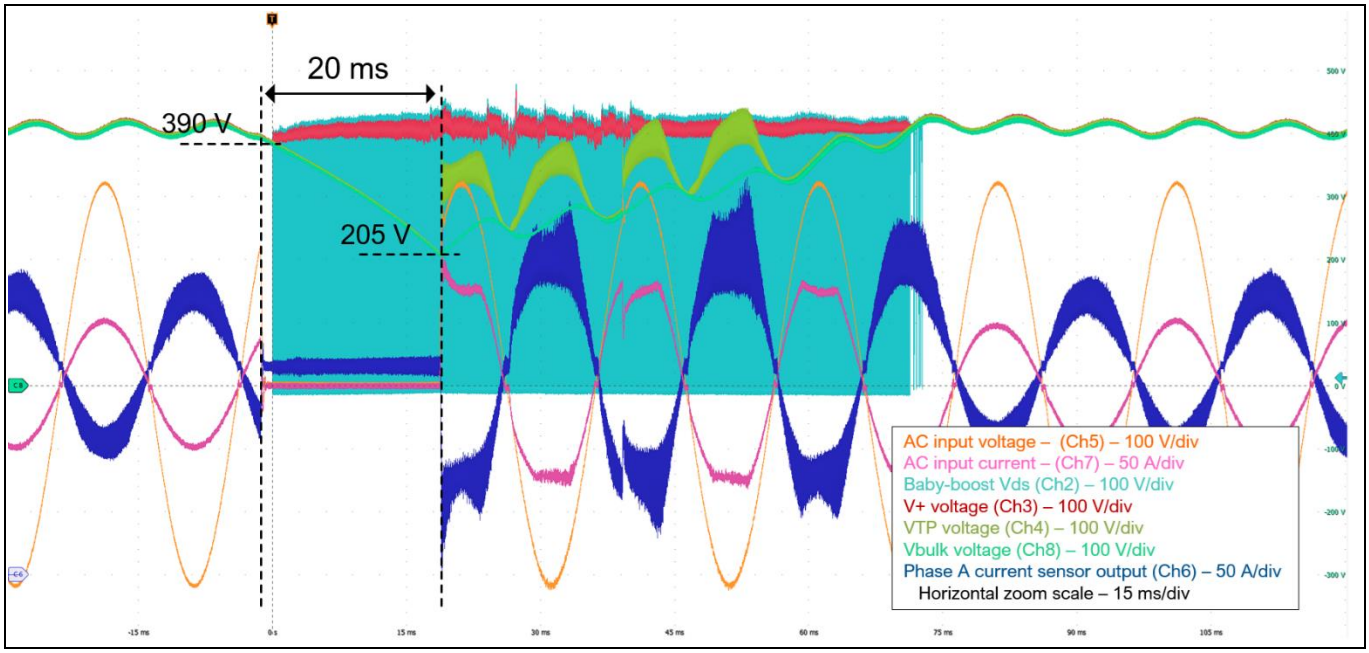


Figure 68 Hold-up time at 100% of the rated load with LCDO duration ≤20 ms

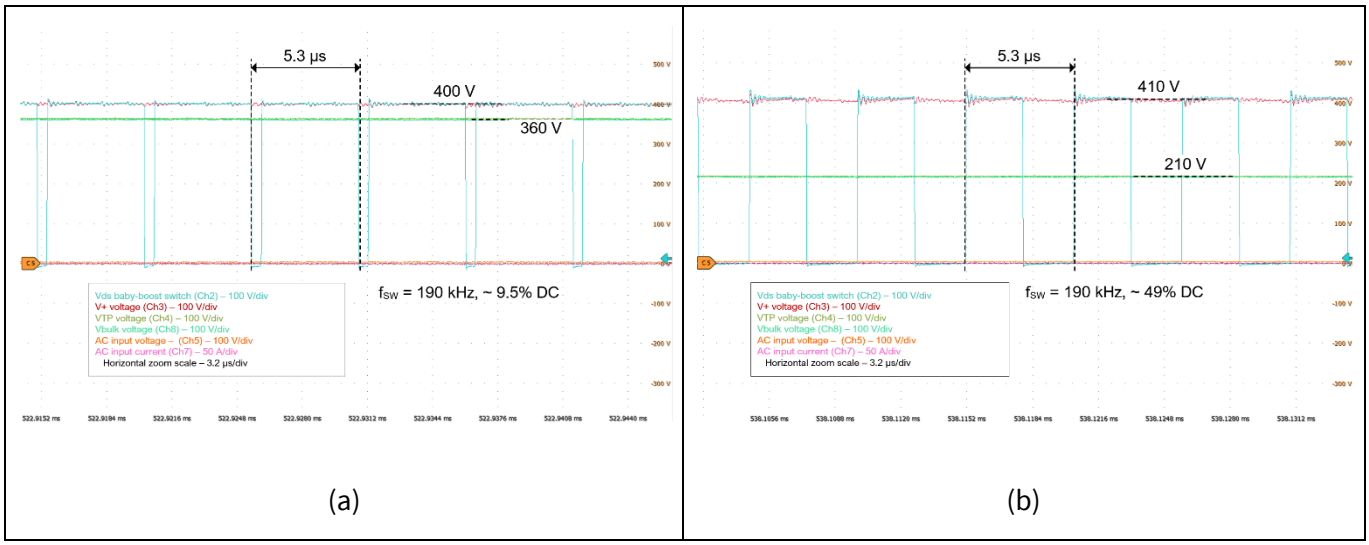


Figure 69 Detail of baby-boost V_{DS}, V_{bulk}, and V_+ waveforms during an LCDO event, 4.3 ms (a) and 20 ms (b) after grid drop event

4.3 EMI measurements

The conducted electromagnetic interference (EMI) of the full PSU was measured with the setup shown in Figure 70. The setup is not certified according to EN 55032. However, the results are valid for a preliminary assessment of the EMI compliance of the unit.

The load used for the test is a passive resistive load. The equipment used is LISN Schwarzbeck NNLK 8129-2 HV, AC source ITECH IT900P, Spectrum analyzer Rigol RSA 3030N, DC load Chroma CHR63215E-600-1050. Spectra have been measured with 9 kHz resolution bandwidth from 150 kHz to 30 MHz as per EN 55032.

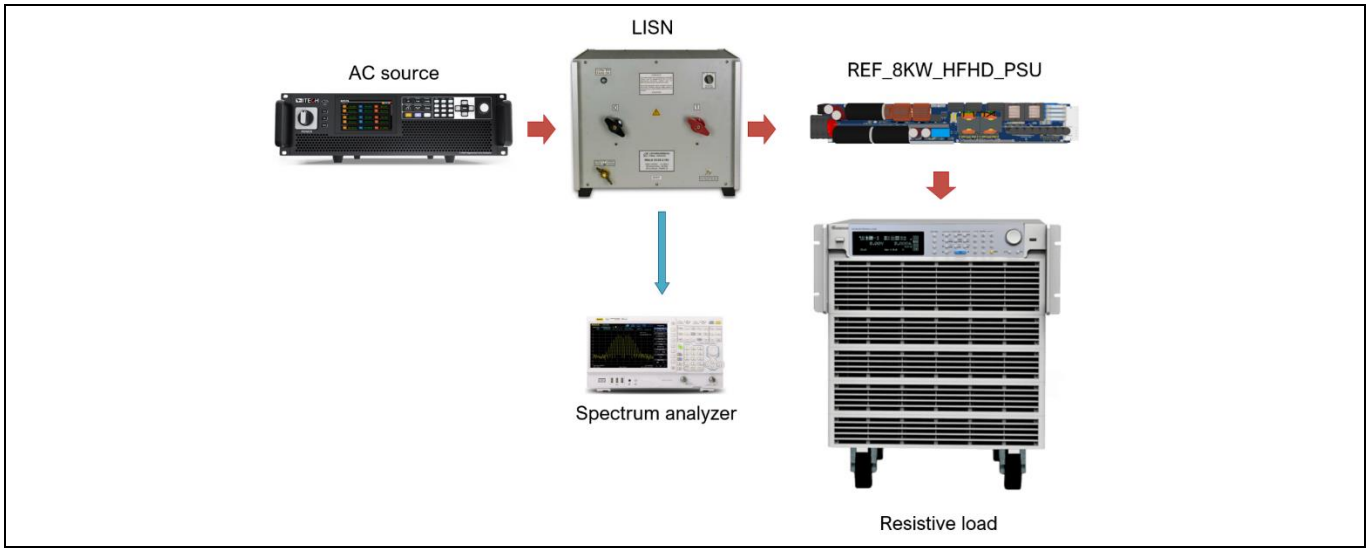


Figure 70 Setup used for EMI test

With the setup discussed, noise floor has been observed even with the DUT connected but not powered. The measured noise floor has been then measured and reported in Figure 71. It is important to notice that the ≥40 dBµV noise floor at frequencies above 8 MHz is related to the setup itself and not on the DUT. Therefore, the noise measured in Figure 72 in this frequency range has been considered as unrelated to the DUT, but rather to be on the setup.

The EMI tests were performed for both line and neutral inputs, with 230 V_{AC} and 8 kW output power. Figure 72 shows the results of the average (AVG) and the positive-peak measurements at 230 V_{AC}. REF_8KW_HFHD_PSU is fully compliant with Class A limits in both quasi-peak and average measurements, also considering that for QP measurements, the equipment used is measuring positive peak at the LISN output, which is expected to return higher values compared to the quasi-peak of the standard.

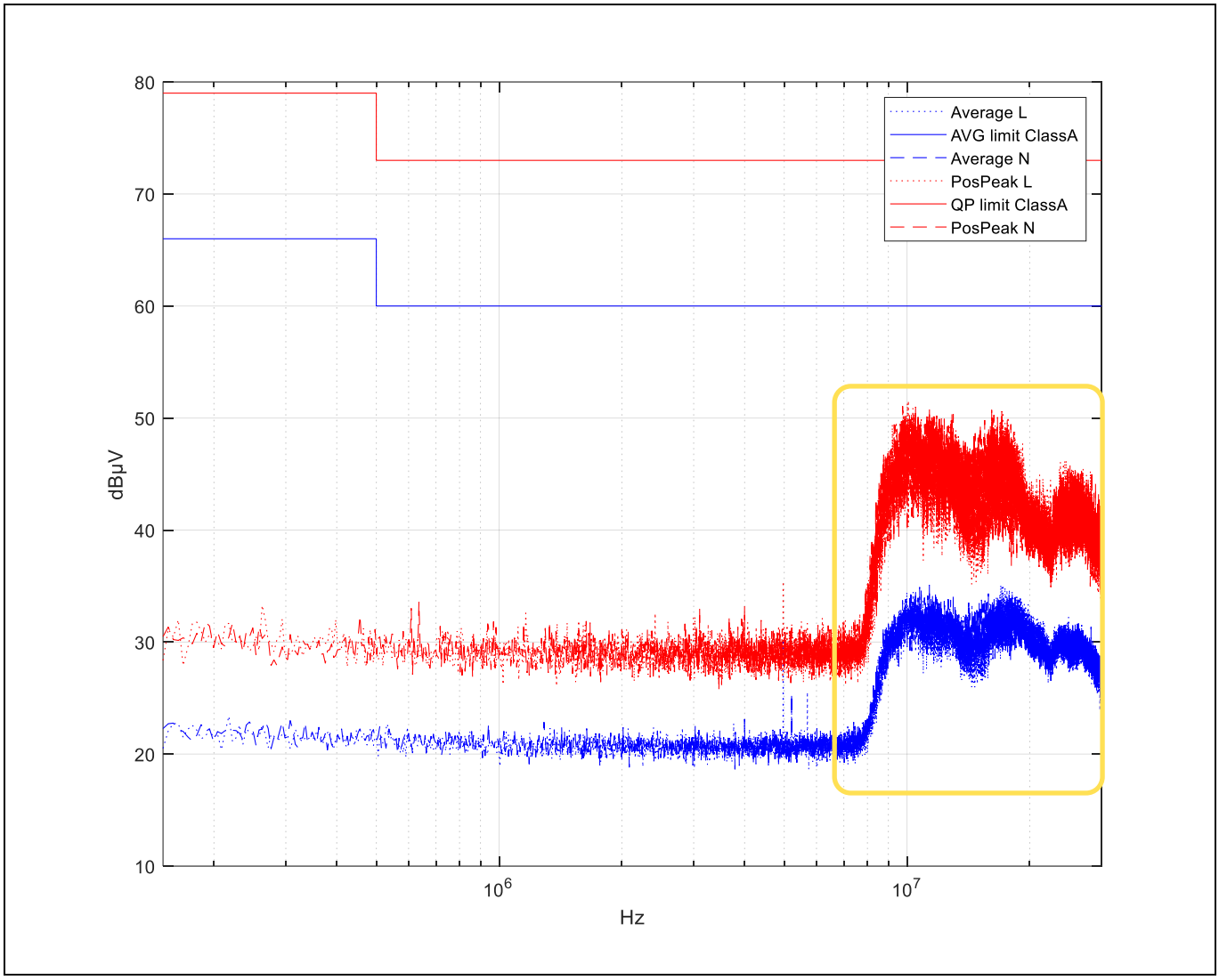


Figure 71 Noise floor in EMI setup measured with DUT connected and OFF, and EN 55032 limits

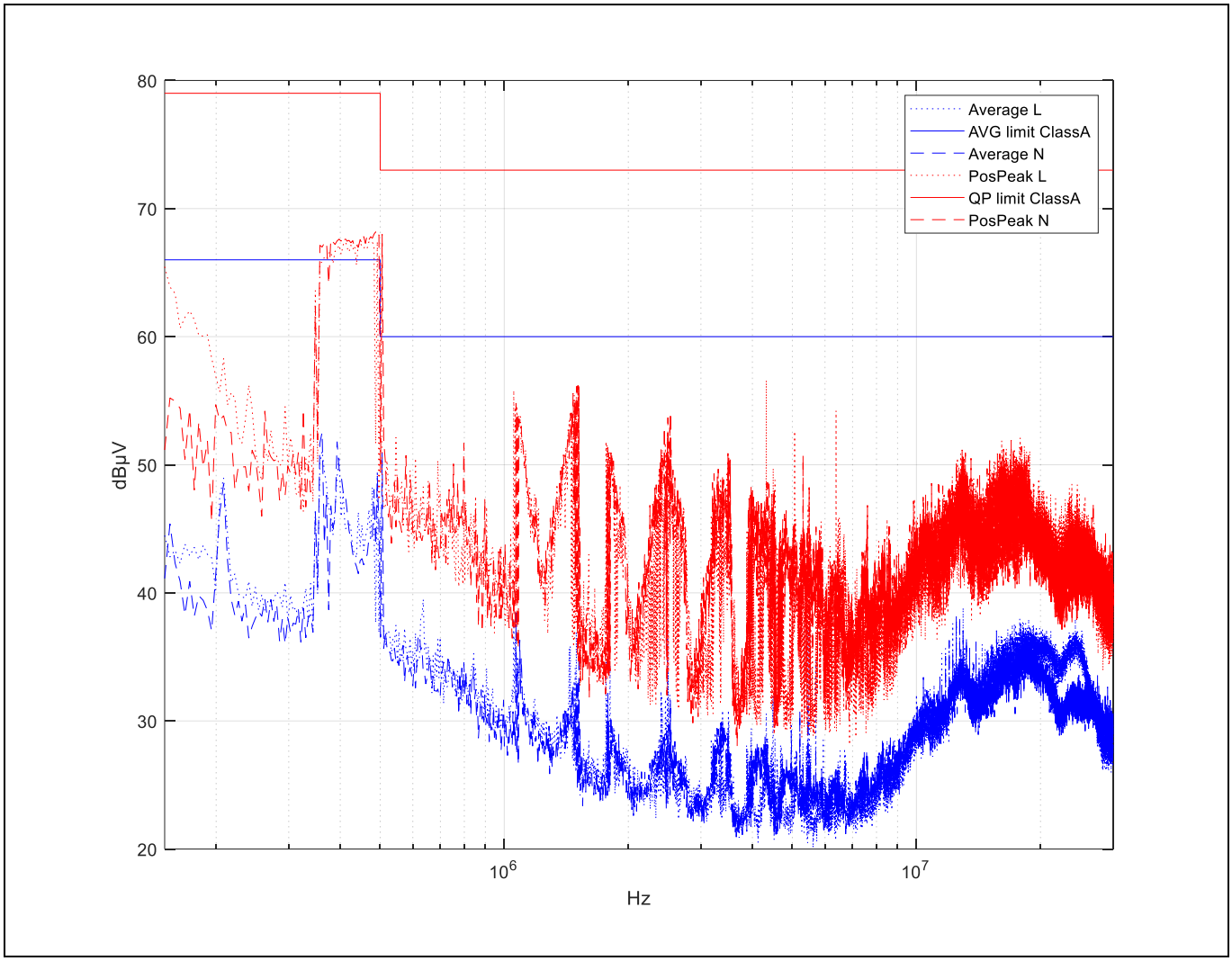


Figure 72 EMI measurements of the DUT at 230 V_{AC} - 8 kW, and EN 55032 limits

5 Summary

This document provides a complete system solution from Infineon designed for AI data center and server PSU applications.

The solution incorporates a bridgeless interleaved totem-pole PFC converter and a DC-DC isolated full-bridge LLC converter, achieving a peak efficiency of 97.5%, and a minimum full load efficiency of 96.5% at 230 V_{AC} including fan power consumption. The efficiency results are obtained with an unprecedented power density of 100 W/in^3.

The REF_8KW_HFHD_PSU reference board utilizes CoolSiC™ 650 V, 600 V CoolMOS™ MOSFETs, and CoolGaN™ power transistors in TOLL packages, and OptiMOS™ 6, all from Infineon. This combination of CoolSiC™, CoolMOS™, CoolGaN™, and OptiMOS™ MOSFETS enables high performance within a compact form factor, as detailed in this document.

The bridgeless PFC topology and the half-bridge LLC incorporate full digital control through an XMC™ 4000 series microcontroller from Infineon.

Note that the PSU's performance excels not only in steady-state conditions, offering high efficiency, but also meets power line disturbance and hold-up time requirements with additional hold-up time boost converter, which can achieve the required 20 ms hold-up at full load.

6 List of figures

FIGURE 1 OVERVIEW OF THE REF_8KW_HFHD_PSU POWER SUPPLY UNIT 1
FIGURE 2 REF_8KW_HFHD_PSU MEASURED EFFICIENCY INCLUDING FAN POWER CONSUMPTION 2
FIGURE 3 DIMENSIONS OF THE 8 KW POWER SUPPLY REF_8KW_HFHD_PSU COMPARED TO OCP V3 REQUIREMENT FOR THE 5.5 KW PSU 8
FIGURE 4 TOP-SIDE PICTURE OF THE REF_8KW_HFHD_PSU WITHOUT CHASSIS 12
FIGURE 5 SIMPLIFIED SCHEMATIC OF REF_8KW_HFHD_PSU (EMI FILTERS NOT SHOWN)....12
FIGURE 6 HARDWARE IMPLEMENTATION OF REF_8KW_HFHD_PSU (TOP SIDE)....16
FIGURE 7 HARDWARE IMPLEMENTATION OF REF_8KW_HFHD_PSU (BOTTOM SIDE) 16
FIGURE 8 OVERVIEW OF THE LLC POWER DAUGHTER CARD....17
FIGURE 9 OVERVIEW OF THE PFC POWER DAUGHTER CARD 17
FIGURE 10 OVERVIEW OF THE LLC XFMR (TRANSFORMER) STRUCTURE 18
FIGURE 11 REF_8KW_HFHD_PSU'S MEASURED EFFICIENCY INCLUDING FAN POWER CONSUMPTION 19
FIGURE 12 REF_8KW_HFHD_PSU'S MEASURED EFFICIENCY INCLUDING FAN POWER CONSUMPTION 19
FIGURE 13 SIMPLIFIED SCHEMATIC OF THE PFC STAGE IN REF_8KW_HFHD_PSU 20
FIGURE 14 PFC EFFICIENCY AND POWER LOSSES STANDALONE AT 230 V AC INPUT VOLTAGE 21
FIGURE 15 BREAKDOWN OF THE PFC LOSSES 21
FIGURE 16 SCHEMATIC OF THE INPUT EMI FILTER 22
FIGURE 17 EMI INPUT FILTER INDUCTOR (A) AND DIFFERENTIAL FLUX DIRECTION (B) 22
FIGURE 18 EMI COMMON MODE INDUCTOR DETAILS (A) AND PINOUT (B) 23
FIGURE 19 3D EXPLOSION DRAWING OF THE EMI FILTER INDUCTOR AND A WINDING EXAMPLE 23
FIGURE 20 PFC INDUCTOR PICTURE (A) AND SPECIFICATIONS (B)....24
FIGURE 21 STAGE CURRENT (A), AND INPUT CURRENT AT THE TOTEM-POLE STAGE INPUT (B) OVER A SINGLE AC LINE CYCLE AT 230 V AC 24
FIGURE 22 CORE HIGH FREQUENCY FLUX (A), AND TOTAL FLUX INCLUDING AC LINE COMPONENT (B) OVER A SINGLE AC LINE CYCLE AT 230 V AC....25
FIGURE 23 PFC INDUCTOR EFFECTIVE INDUCTANCE VS DC BIAS AND BULK CAPACITANCE RIPPLE OVER A SINGLE AC LINE CYCLE AT 230 V AC 25
FIGURE 24 CURRENT LOOP STRUCTURE WITH DETAILS OF LOAD AND DUTY-CYCLE FEED-FORWARD (DFF) 26
FIGURE 25 SENSING CIRCUITRY OF THE TOTEM-POLE PFC CONVERTER WITH XMC™ 27
FIGURE 26 DRIVING COOLSIC™ IN THE FAST-SWITCHING BRIDGE....28
FIGURE 27 DRIVING COOLSIC™ IN THE RECTIFICATION BRIDGE....28
FIGURE 28 REGULATED SUPPLY VOLTAGE FOR HF AND LF BRIDGES BOOTSTRAPPING 29
FIGURE 29 HIGH SIDE BOOTSTRAP CAPACITOR VOLTAGE OF THE HF BRIDGE – (A) STAGE A (B) LF BRIDGE, BOTH DURING ONE AC LINE CYCLE 29
FIGURE 30 SIMPLIFIED SCHEMATIC OF THE LLC DC/DC CONVERTER IN REF_8KW_HFHD_PSU....30
FIGURE 31 LLC DC/DC STANDALONE: EFFICIENCY AND POWER LOSSES AT 400 V INPUT....31
FIGURE 32 POWER LOSS BREAKDOWN FOR THE LLC DC-DC STAGE AT 100% OF RATED POWER....31
FIGURE 33 POWER LOSS BREAKDOWN FOR THE LLC DC-DC STAGE AT 50% OF RATED POWER....32
FIGURE 34 DETAILED STACK-UP OF XFMR A (TRANSFORMER AND PARALLEL RESONANT INDUCTOR B INTEGRATED) 33
FIGURE 35 DETAILED STACK-UP OF XFMR B (TRANSFORMER, SERIES, AND PARALLEL RESONANT INDUCTORS A INTEGRATED) 33
FIGURE 36 INTEGRATED PLANAR TRANSFORMER ASSEMBLY: TOP VIEW (A) AND SIDE VIEW (B) 34
FIGURE 37 AN OVERVIEW OF THE PRIMARY- AND SECONDARY-SIDE WINDING PCBS....35
FIGURE 38 DETAIL OF THE PRIMARY SIDE PCB: WINDING ARRANGEMENT FOR EACH BOARD 35
FIGURE 39 DETAIL OF THE SECONDARY SIDE PCB: WINDING ARRANGEMENT FOR EACH BOARD....35
FIGURE 40 DRIVING COOLGAN™ ON THE PRIMARY SIDE OF THE LLC CONVERTER 36
FIGURE 41 BIASING OF THE HIGH-SIDE DRIVER FOR COOLGAN™ DRIVING....36
FIGURE 42 DRIVING OPTIMOS™ ON THE SECONDARY SIDE OF THE LLC CONVERTER....37
FIGURE 43 SCHEMATIC OF THE BABY-BOOST CIRCUITY ON THE MAIN BOARD TO COMPLY WITH LCDO REQUIREMENT 38
FIGURE 44 BABY-BOOST OPERATION DURING LCDO EVENT AT 100% LOAD 39
FIGURE 45 MEASURED EFFICIENCY (A) AND POWER LOSSES (B) OF REF_8KW_HFHD_PSU FOR DIFFERENT INPUT LINE VOLTAGES (180 V_{AC}, 230 V_{AC}, AND 277 V_{AC}), FAN POWER CONSUMPTION INCLUDED....40
FIGURE 46 POWER FACTOR (PF) OF THE PSU AND OCP POWER FACTOR LIMIT....41
FIGURE 47 INPUT CURRENT TOTAL HARMONIC DISTORTION (ITHD) OF THE PSU AND OCP ITHD LIMIT 41
FIGURE 48 PSU STARTUP AT 230 V_{AC} INPUT, FULL LOAD....42
FIGURE 49 LLC CONVERTER STARTUP....42

List of figures

FIGURE 50 LLC RESONANT AND PFC CURRENTS, AND OUTPUT AND BULK VOLTAGES AT 100% LOAD, 230 V_{AC} 43
FIGURE 51 BULK VOLTAGE RIPPLE AT 100% LOAD, 230 V_{AC} (A) AND 277 V_{AC} INPUT VOLTAGE (B) 44
FIGURE 52 PSU OUTPUT VOLTAGE RIPPLE AT 100% LOAD 44
FIGURE 53 PFC STEADY-STATE OPERATION AT 230 V_{AC}, FULL LOAD 45
FIGURE 54 PFC STEADY-STATE OPERATION AT 180 V_{AC}, FULL LOAD 45
FIGURE 55 PFC ZERO CROSSING A 46
FIGURE 56 PFC ZERO CROSSING B 46
FIGURE 57 LLC WAVEFORMS DURING STEADY-STATE OPERATION, FULL LOAD, 230 V_{AC} INPUT, V_{BULK} AT MINIMUM PEAK OF THE DOUBLE LINE FREQUENCY RIPPLE (395 V) 47
FIGURE 58 LLC WAVEFORMS DURING STEADY-STATE OPERATION, FULL LOAD, 230 V_{AC} INPUT, V_{BULK} AT MAXIMUM PEAK OF THE DOUBLE LINE FREQUENCY RIPPLE (420 V) 47
FIGURE 59 PSU AIRFLOW DIRECTION 48
FIGURE 60 AIRFLOW VELOCITY MAGNITUDE - CROSS SECTION CLOSE TO PSU CEILING 48
FIGURE 61 AIRFLOW VELOCITY MAGNITUDE - CROSS SECTION AT PSU CENTER 48
FIGURE 62 PSU REPETITIVE LOAD TRANSIENT, 10-100% AND 100-10% OUTPUT LOAD 49
FIGURE 63 PSU LOAD TRANSIENT AT 10-90% (A) AND 90-10% (B) OUTPUT LOAD, DETAILED VIEW 49
FIGURE 64 PSU LOAD TRANSIENT AT 10-50% (A) AND 50-10% (B) OUTPUT LOAD, DETAILED VIEW 50
FIGURE 65 AC INPUT VOLTAGE SAG, 230 V_{AC} TO 180 V_{AC}, 100% OUTPUT LOAD 50
FIGURE 66 AC INPUT VOLTAGE SAG, 230 V_{AC} TO 160 V_{AC}, 100% OUTPUT LOAD 51
FIGURE 67 HOLD-UP TIME AT 100% OF THE RATED LOAD WITH LCDO DURATION >20 MS 51
FIGURE 68 HOLD-UP TIME AT 100% OF THE RATED LOAD WITH LCDO DURATION ≤20 MS 52
FIGURE 69 DETAIL OF BABY-BOOST V_{DS}, V_{BULK}, AND V_+ WAVEFORMS DURING AN LCDO EVENT, 4.3 MS (A) AND 20 MS (B) AFTER GRID DROP EVENT 52
FIGURE 70 SETUP USED FOR EMI TEST 53
FIGURE 71 NOISE FLOOR IN EMI SETUP MEASURED WITH DUT CONNECTED AND OFF, AND EN 55032 LIMITS 54
FIGURE 72 EMI MEASUREMENTS OF THE DUT AT 230 V_{AC} - 8 KW, AND EN 55032 LIMITS 55
FIGURE 73 SCHEMATIC OF THE MAIN BOARD (M100001428) – PAGE 1 65
FIGURE 74 SCHEMATIC OF THE MAIN BOARD (M100001428) – PAGE 1 66
FIGURE 75 SCHEMATIC OF THE PFC POWER BOARD (PW200001428) 67
FIGURE 76 SCHEMATIC OF THE LLC POWER BOARD (PW100001427) 68
FIGURE 77 SCHEMATIC OF THE LLC CONTROL BOARD (CD100001427) 69
FIGURE 78 SCHEMATIC OF THE LLC SECONDARY SIDE WINDING EMBEDDING THE SR BRIDGE (MG100001429) 70

7 Bill of materials

Table 6 Bill of materials for the main board M100001428

Designator	Value	Tolerance	Description
C1, C2, C13, C14	4.7 nF	Y2	Capacitor ceramic
C3, C4, C37, C54	100 nF	X7R	Capacitor ceramic
C5, C79, C80, C88, C96, C98, C100, C102, C105, C107, C110, C113, C114	100 nF	X7R	Capacitor ceramic
C6, C26, C30, C55, C87	100 pF	X7R	Capacitor ceramic
C7	10 µF	10%	Capacitor foil
C8, C9, C10	1.5 µF X2	10%	Capacitor foil
C11, C12, C35	2.2 µF X2	10%	Capacitor foil
C15, C16, C17	1000 µF	20%	Capacitor polarized
C18, C19, C20, C21	100 µF	20%	Capacitor polarized
C22, C23, C24, C25, C27, C28, C29, C31, C32, C34, C117	1 µF	X7R	Capacitor ceramic
C33, C36	4.7 µF	X8L	Capacitor ceramic
C38, C39, C40, C41, C42, C43, C44, C45, C67, C68	33 nF	5%	Capacitor ceramic
C46, C47, C48, C49, C50, C51, C52, C53	820 µF	20%	Capacitor electrolytic
C56	2.2 µF	5%	Capacitor foil
C57, C58, C89, C90, C91, C92, C93, C94, C95, C115, C116, C120	330 pF	X7R	Capacitor ceramic
C84, C85, C111, C112	10 pF	X7R	Capacitor ceramic
C97, C99, C101, C104, C106, C108, C109	10 µF	X5R	Capacitor ceramic
C103	10 µF	X5R	Capacitor ceramic
C118, C119	10 µF	X7R	Capacitor ceramic
D1, D2	IDL12G65C5	–	Schottky diode
D3, D4	S8KCDICT	–	Standard diode
D5	BAT165	–	Schottky diode
D6	ORANGE LED	–	LED
D7	BLUE LED	–	LED
D8	DFLS1200	–	Diode
F1, F2, F3, F4	30 A	–	AC input fuse
GDT1	SL1002A600SP	–	GDT - Surge arrester
H1, H7	HT200001426	–	Heatsink
H2	HT300001426	–	Heatsink
H4	HT500001426	–	Heatsink
H5	HT400001426	–	Heatsink
IC1, IC13, IC14	1EDN8511B	–	Integrated circuit
IC2, IC4	MCR1101-50-3	–	Hall sensor

Designator	Value	Tolerance	Description
IC3, IC5	1EDB8275F	–	Integrated circuit
IC6	LM5050-1	–	O-ring gate driver IC
IC7	4DIR1400H	–	Integrated circuit
IC8	LV3842X	–	Gate driver IC
IC9	TLV1391IDBVR	–	TLV1391: Single differential comparators
IC10	TLV2376IDR	–	Integrated circuit
IC11	XMC4200-Q48K256	–	Integrated circuit
L1, L2	0.5 mH	–	Common mode choke
L3	30 µH	–	Buffer choke
L4, L5	157 µH	–	Pfc-choke
L7	22 µH	–	Magnetic
L8	Ferrite bead 60 Ω at 100 MHz	–	Magnetic
MOV1, MOV2	V320LA20AP	–	Varistor
NTC1, NTC2, NTC3	5R	20%	NTC resistor
PW100001427	–	–	Pin header, 26 contacts
PW200001427	–	–	Pin header, 19 contacts
Q1, Q2, Q3, Q6, Q7	IPT60R016CM8	–	NMOSFET
Q4, Q5	IPT60R050G7	–	NMOSFET
Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q15, Q16, Q17	ISC018N08NM6	–	N-channel MOSFET
R1, R4, R6, R9, R14, R17, R40, R42	4R7	1%	Resistor
R2	33R	1%	Resistor
R3	1.5R	1%	Resistor
R5, R8, R15, R18, R41, R43, R47, R67, R72	510R	1%	Resistor
R7, R73	22R	1%	Resistor
R10	22k1	0.1%	Resistor
R11, R12, R20, R22, R23, R24, R25, R34, R35, R36, R37, R63, R70, R71	15k	1%	Resistor
R13, R16	10R	1%	Resistor
R19	100R	1%	Resistor
R21	100u	1%	Resistor
R48, R55, R56, R57, R59, R62	309k	0.1%	Resistor
R49, R50, R51, R52, R58, R74	10k	0.1%	Resistor
R53, R54, R60, R61	17k8	0.1%	Resistor
R64, R66	1K1	1%	Resistor
R65	51k	0.1%	Resistor
R68, R69	2k7	1%	Resistor

Designator	Value	Tolerance	Description
R75	33k	1%	Resistor
R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91	309k	0.1%	Resistor
T1	TF200001427	–	PWR transformer
T2	TF100001427	–	PWR transformer
TR1	MG600003070	–	Current sense transformer
TR2	XT01	–	Common mode power line choke
X1	TE-2391130-4	–	Female header, 2 contacts
X2	–	–	Female Header, 26 Contacts 2 mm
X5	FTSH-105-01-L-DV-K	–	Connector
XTAL1	QT325S-12.000MEEQ-T	–	Crystal oscillator

Table 7 Bill of materials for the PFC power card PW200001428

Designator	Value	Tolerance	Description
C1, C2, C7, C8, C13, C14, C20, C23	100 pF	X7R	Capacitor ceramic
C3, C9, C15, C21	100 nF	X7R	Capacitor ceramic
C4, C5, C6, C10, C11, C12, C16, C17, C18, C22, C32, C34, C35, C36, C37, C39, C40, C41	4.7 µF	X7R	Capacitor ceramic
C19, C26	150 µF	20%	Capacitor polarized
C24	33 µF	10%	Capacitor polarized
C25, C33	1 nF	X7R	Capacitor ceramic
C27, C28, C29, C30, C31, C38	100 nF	X7R	Capacitor ceramic
D1, D2, D3, D4, D5, D6, D12, D16, D17, D18, D19, D20, D21	BAT165	–	Diode, SOD323
D7, D8, D9, D15, D23	ES1JAL_M3G	–	Diode
D10, D11, D13, D14	DFLS1200-F	–	Schottky diode
D22	SMAJ130A-E3/61	–	Zener diode
IC1, IC2, IC3	2EDB9259Y	–	Dual-channel isolated gate driver
IC7	TLV431B	0.5%	TLV431B - Adjustable precision shunt regulator 0.5%
IC8	ICE2QR2280G	–	Integrated circuit
IC9	VOL617A-3	–	Integrated circuit
IC10	1EDN8511B	–	Integrated circuit

Designator	Value	Tolerance	Description
IC11	LM317EMP/NOPB	–	Integrated circuit
Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8	IMT65R040M2H	–	GIT GaN transistor
Q9, Q10, Q11, Q12	IMT65R015M2H	–	GIT GaN transistor
R1, R2, R5, R6, R9, R10, R13, R14	2R2	1%	Resistor
R3, R4, R7, R8, R11, R12, R15, R16	1R	1%	Resistor
R17, R18, R21, R22	1k0	1%	Resistor
R19, R20, R23, R24	10R	1%	Resistor
R25, R26, R29, R30, R33, R34, R50	510R	1%	Resistor
R27, R31, R35, R52	1k18	1%	Resistor
R28, R32	4R7	1%	Resistor
R36	10R	1%	Resistor
R37	33R	1%	Resistor
R47	15k	1%	Resistor
R48	3k6	1%	Resistor
R49, R51	825R	1%	Resistor
R53	2K7	1%	Resistor
R54	2R2	1%	Resistor
R55	43k	1%	Resistor
R56	12k	1%	Resistor
R57	3k48	1%	Resistor
R58	46k4	1%	Resistor
R59	10K NTC	3%	Resistor
TF1	8032.0205.024 Rev1	–	Transformer

Table 8 Bill of materials for the LLC power card PW100001427

Designator	Value	Tolerance	Description
TR1, TR3	XT01	–	Common mode power line choke
R44	10k	1%	Resistor
R12	10K NTC	3%	Resistor
R10, R13, R21, R22, R45	33k	1%	Resistor
R8, R9, R14, R19, R20, R23	10R	1%	Resistor
R6, R7, R17, R18, R32, R33, R46, R48	511R	1%	Resistor
R3, R4, R11, R15, R25, R27, R28, R30	2R7	1%	Resistor
R1, R2, R5, R16, R24, R26, R29, R31	10R	1%	Resistor
Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8	IGT65R035D2	–	GaN transistor
L1, L2, L3, L4, L5, L6, L7, L8	SRF2012-361YA	–	Common mode power line choke
IC9	1EDN8511B	–	Integrated circuit

Designator	Value	Tolerance	Description
IC2, IC4	1EDN8550B	–	Gate driver IC
IC1, IC3	1EDB8275F	–	Integrated circuit
D1, D10	BAT165	–	Schottky diode
C34	330 pF	X7R	Capacitor ceramic
C22, C23	1.5 pF	C0G	Capacitor ceramic
C21, C31, C32	10 µF	X7R	Capacitor ceramic
C12, C14, C15, C35, C36	100 nF	X7R	Capacitor ceramic
C3, C7, C8, C9, C16, C17, C18, C30	1 µF	X7R	Capacitor ceramic
C2, C5	100 pF	X7R	Capacitor ceramic
C1, C4, C6, C10, C11, C13, C19, C20	2n2	X7R	Capacitor ceramic

Table 9 Bill of materials for the control card CD100001427

Designator	Value	Tolerance	Description
C1, C12, C49, C54, C59, C65, C66, C67, C68, C74, C75	100 nF	X7R	Capacitor ceramic
C2, C3, C4, C5, C6	22 µF	X7R	Capacitor ceramic
C7, C8, C13, C14, C15, C16, C17, C18, C19, C20	10 µF	X7R	Capacitor ceramic
C10, C21	100 nF	X7S	Capacitor ceramic
C48, C55, C56, C69	10 µF	X5R	Capacitor ceramic
C57, C58, C61, C63, C64, C71	330 pF	X7R	Capacitor ceramic
C60, C62	4 nF	X7R	Capacitor ceramic
C70, C72	100 pF	X7R	Capacitor ceramic
D1, D2, D7, D8, D9, D10	BAT165	–	Schottky diode
D3	BAT54-03W	–	Schottky diode
D4	DFLS1200	–	Diode
D11	Green LED	–	LED
IC8	dsPIC33CK256MP203-I/M5	–	MCU
IC10	TLV2376IDR	–	Integrated circuit
IC12	LMH6642MF	–	Integrated circuit
IC13	TLS820D0ELV33XUM	–	Low dropout linear voltage regulator
L1	IHLP4040DER470M5A	–	Magnetic
L2	IHLP4040DZER680M5A	–	Magnetic
L3	Ferrite bead 60 Ω at 100 MHz	–	Magnetic
NTC1	10k	1%	NTC resistor
R1	6k65	1%	Resistor
R2, R47, R53	10k	0.1%	Resistor

Designator	Value	Tolerance	Description
R3	21k	1%	Resistor
R4	130k	1%	Resistor
R5, R48, R56, R63	4k99	0.1%	Resistor
R6	4k59	0.1%	Resistor
R7	75k	1%	Resistor
R8, R31	1k	1%	Resistor
R10	115k	1%	Resistor
R15, R62	2k7	1%	Resistor
R16, R19, R20, R49, R52	124R	0.1%	Resistor
R18, R70	100R	1%	Resistor
R50, R54, R58	49k9	0.1%	Resistor
R51, R55, R59	54k9	0.1%	Resistor
R60, R69	15k	1%	Resistor
R71, R72, R77	510R	1%	Resistor
R73, R74	261R	1%	Resistor
R75	1R0	1%	Resistor
U1, U2	LMR38025SQDRRRQ1	–	Integrated synchronous buck
X1, X2	–	–	Pin header, 5 contacts
X3	TMM-113-03-L-D	–	Pin header, 26 contacts
X6	B2B-ZR	–	Connector

Table 10 Bill of materials for the secondary-side transformer PCB MG100001429

Designator	Value	Tolerance	Description
C2, C3, C4, C5, C6, C7, C8, C9, C10	4.7 µF	X8L	Capacitor ceramic
C13, C14, C15, C16, C17, C18	1 µF	X7R	Capacitor ceramic
D1, D2	BAT46WJ	–	Schottky diode
IC1, IC2	2EDB7259K	–	Gate driver IC
R1, R2	2R2	1%	Resistor
R3, R4, R5, R6, R7, R8, R9, R10	1R	1%	Resistor
R11, R12	2k	1%	Resistor
T1, T2, T3, T4, T5, T6, T7, T8	IQE033N08LM6CG	–	N-Channel MOSFET

8 Schematics

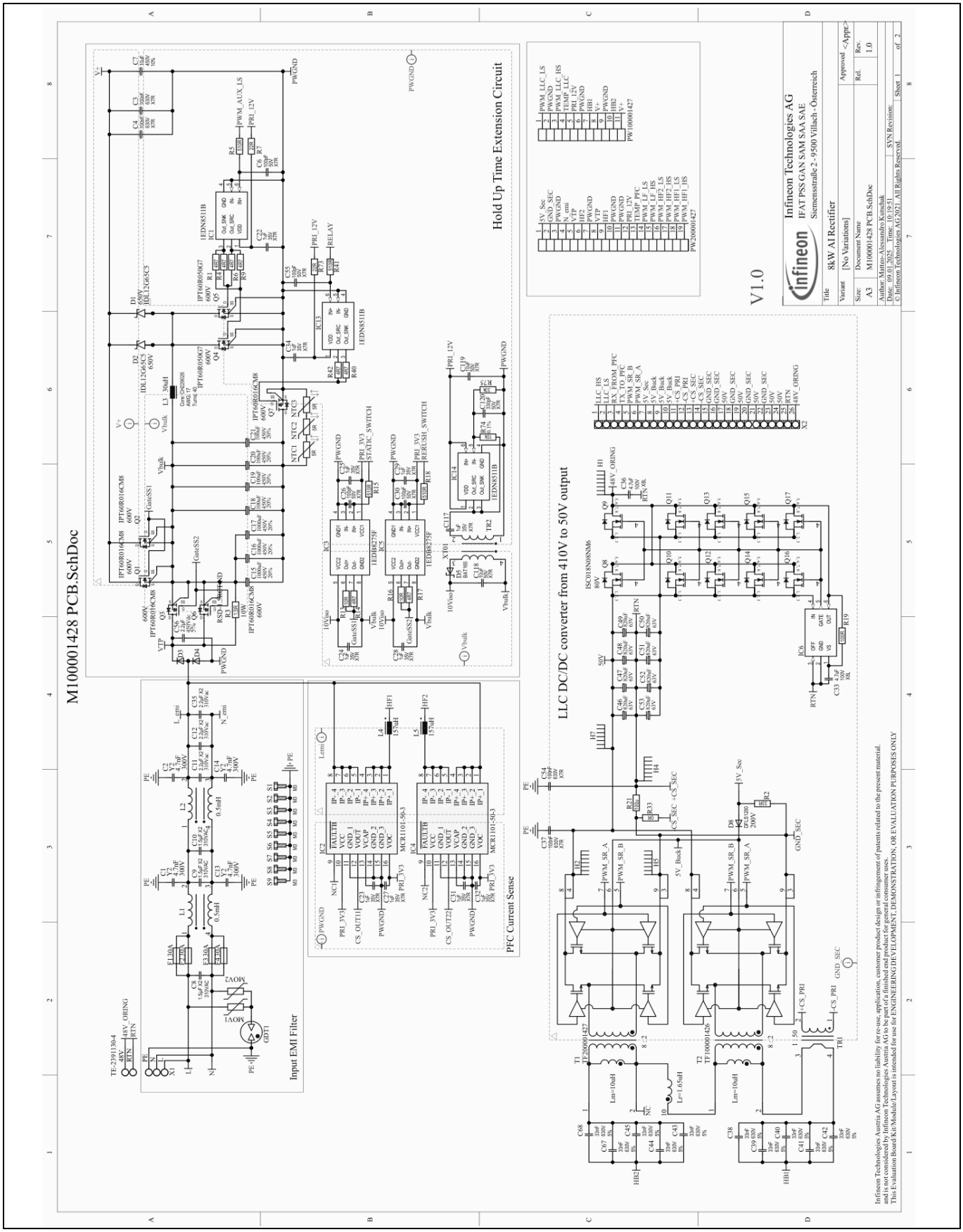


Figure 73 Schematic of the main board (M100001428) – page 1

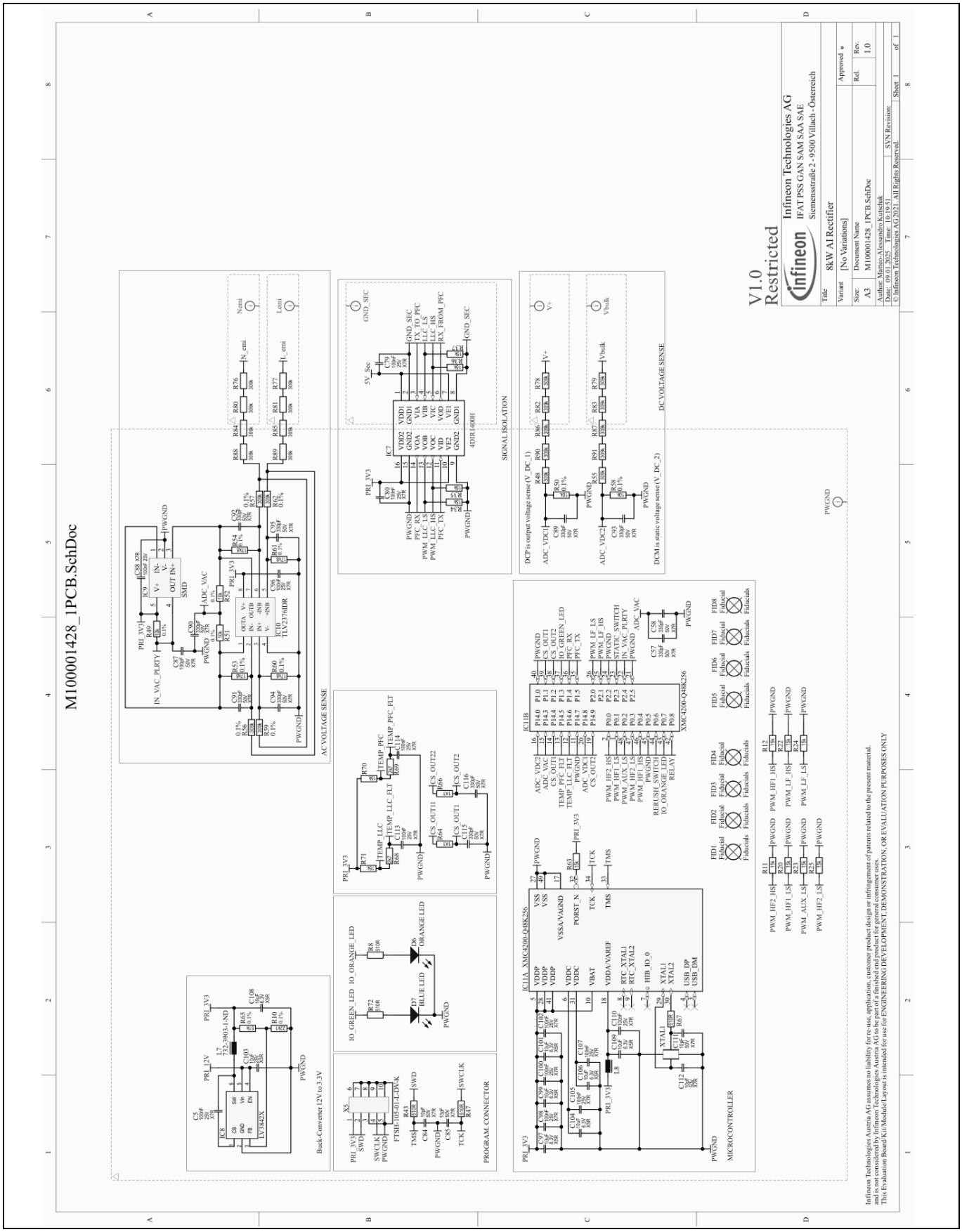


Figure 74 Schematic of the main board (M100001428) – page 1

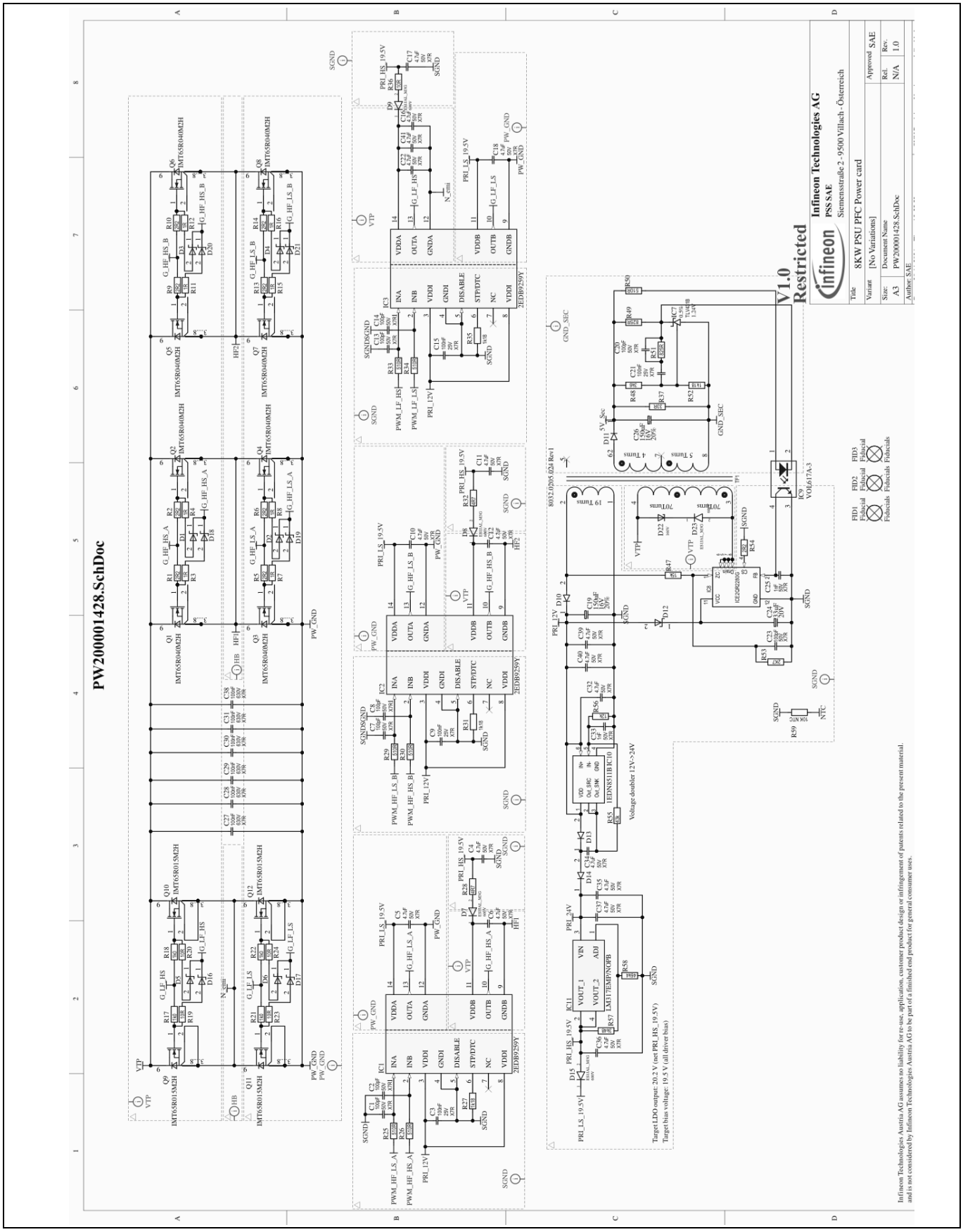


Figure 75 Schematic of the PFC power board (PW200001428)

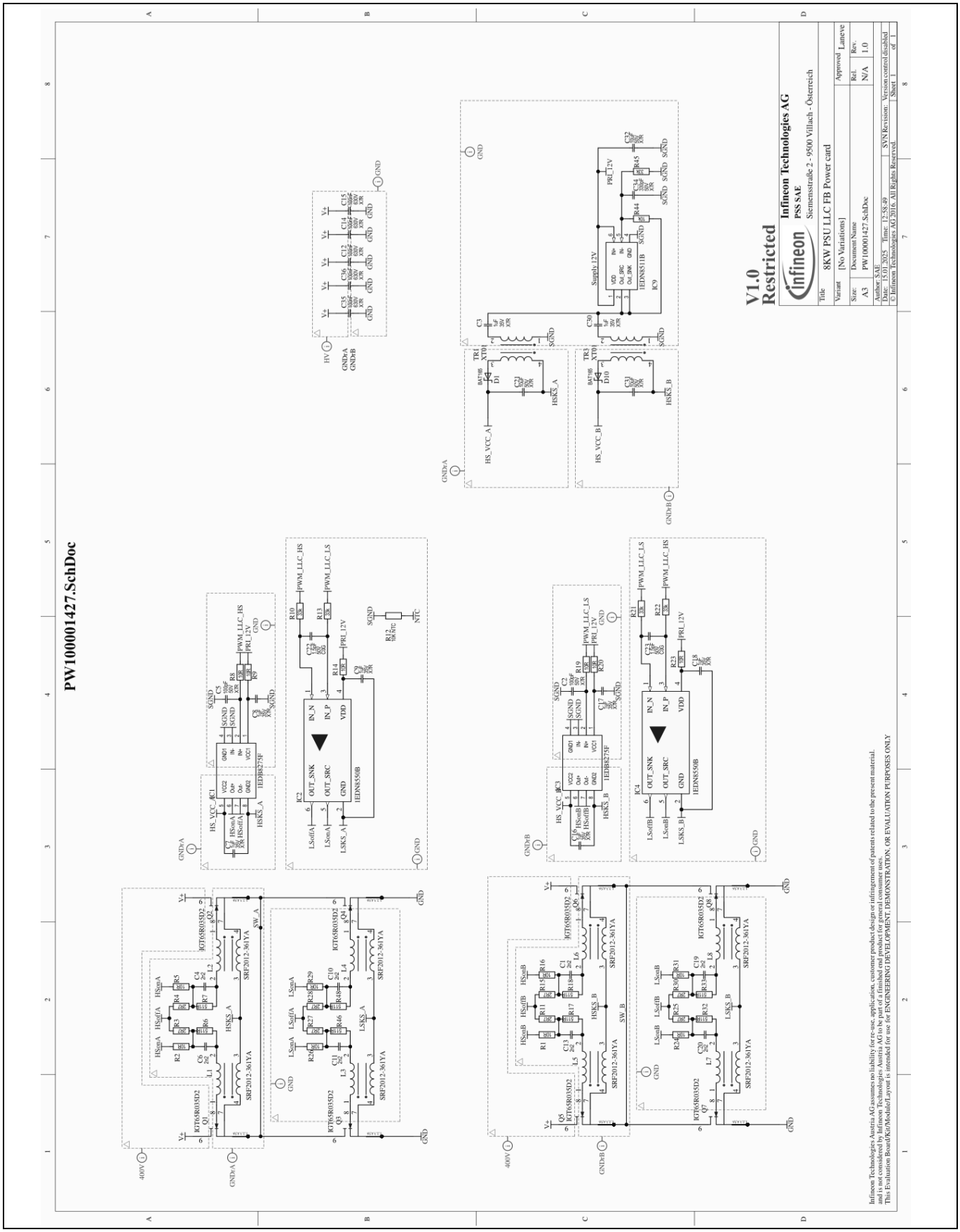


Figure 76 Schematic of the LLC power board (PW100001427)

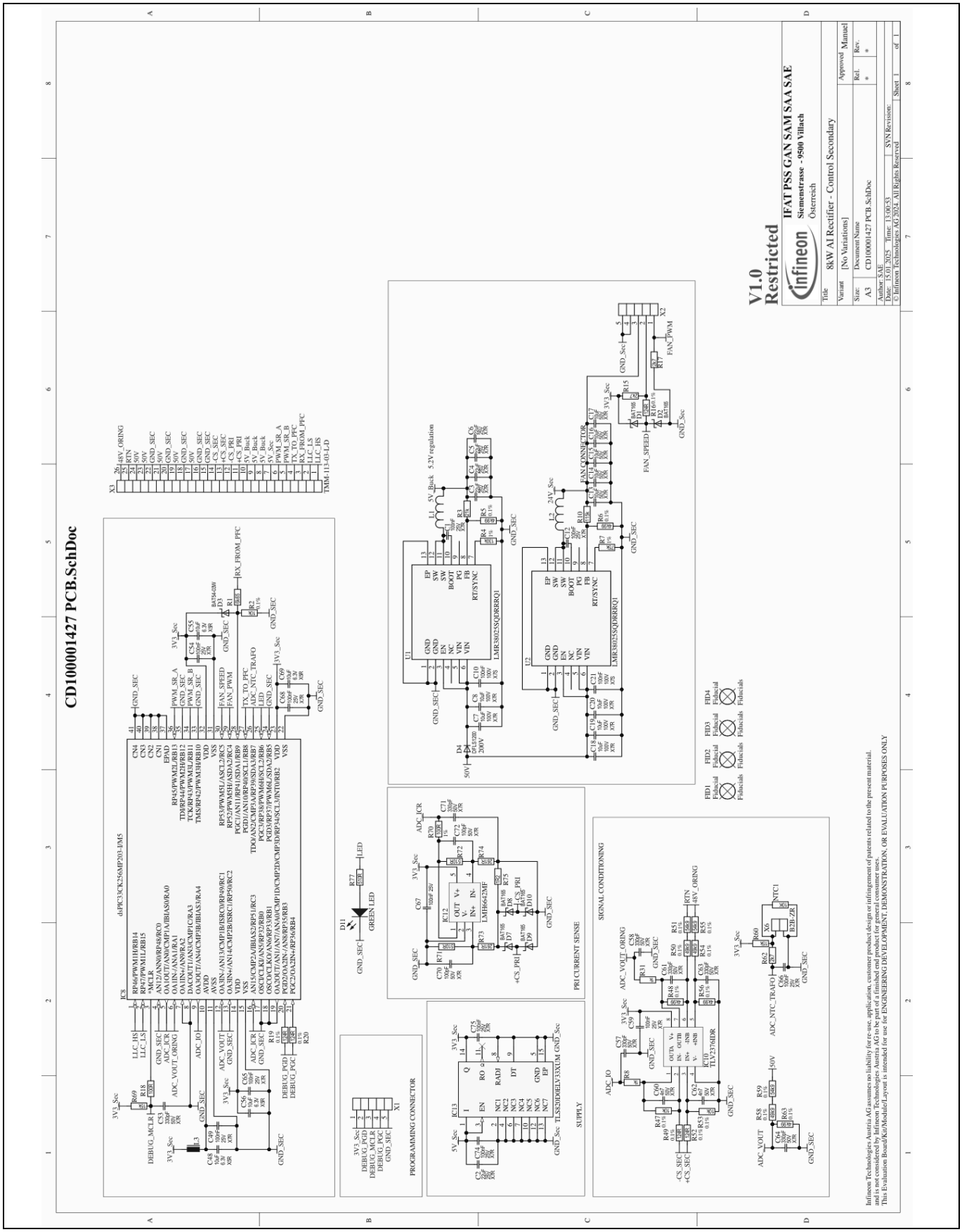


Figure 77 Schematic of the LLC control board (CD100001427)

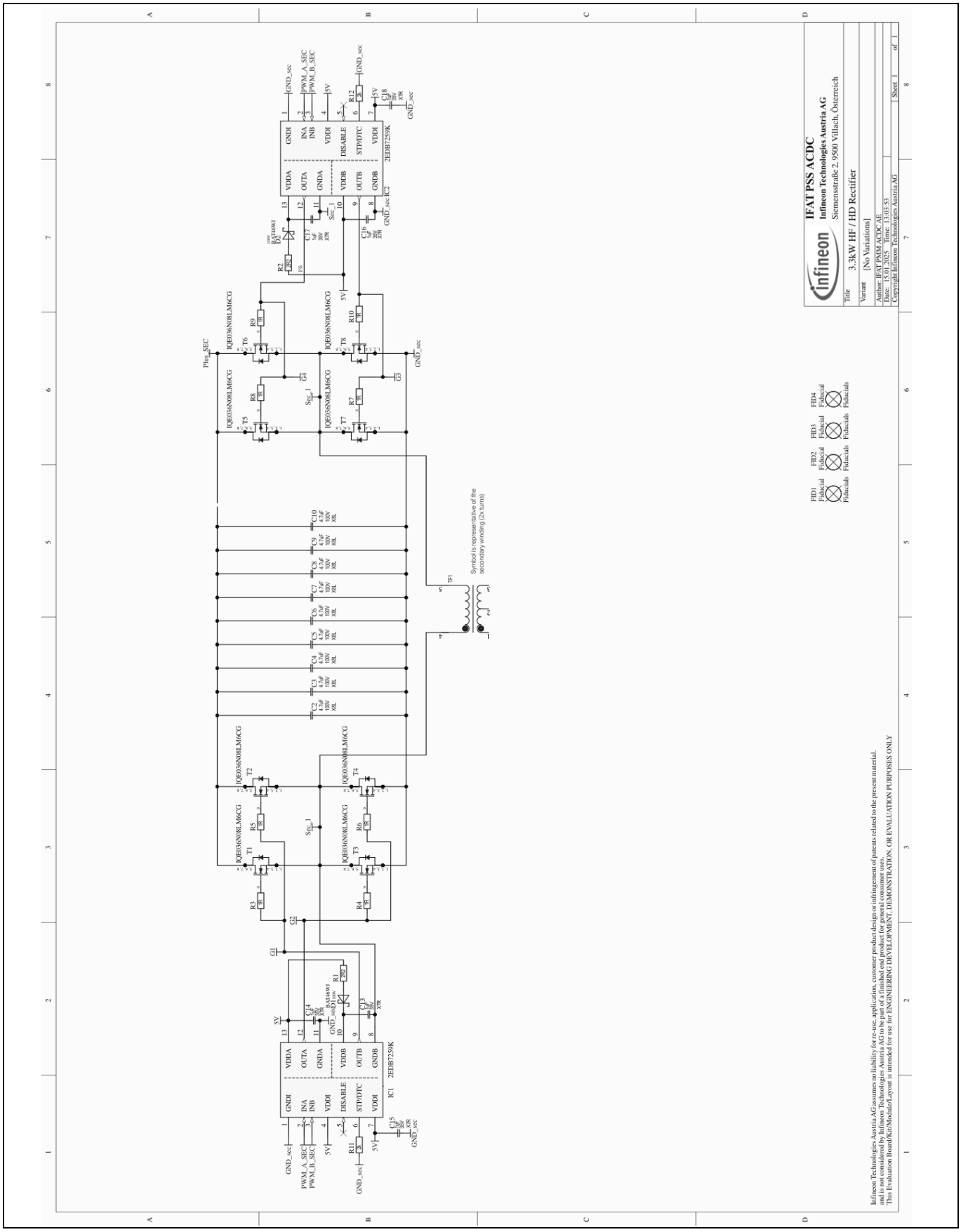


Figure 78 Schematic of the LLC secondary side winding embedding the SR bridge (MG100001429)

References

[1] Open Rack V3 5.5 kW 48V PSU Specification Rev: 1.0, Open Compute Project (OCP)

[2] “Differential-Mode Inductance Integration with Common-Mode EMI Filter,” M. Chen, M. Escudero, M. A. Kutschak, D. Meneses, APEC 2024

[3] “Paralleling power MOSFETs in high current applications,” AN_2009_PL18_2010_105641, Infineon technologies AG

[4] B. Li, Q. Li, F. C. Lee and Y. Yang, “A symmetrical resonant converter and PCB transformer structure for common mode noise reduction,” 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, USA, 2017, pp. 5362-5368, doi: 10.1109/ECCE.2017.8096898.

[5] “How to parallel CoolGaN™ 600 V HEMT in halfbridge configurations for higher-power applications”, Infineon technologies AG, Engineering Report ER_1908_PL52_1910_100139.

[6] REF_3K3W_HFHD_PSU, “3.3 kW high-frequency and high-density PSU for server and datacenter applications,” 2024 Infineon Technologies AG, Application Note AN145544.

Acronyms/abbreviations

Table 11 Acronyms/abbreviations

Acronym	Description
ADC	analog to digital converter
BW	bandwidth
BTM	PCB bottom side
CCM	continuous conduction mode
DFF	duty feed-forward
FB	full-bridge
GaN	gallium nitride
HB	half-bridge
HV	high voltage
IBC	Intermediate bus converter
iTHD	input current total harmonic distortion
LCDO	line cycle drop-out
LDO	low dropout voltage regulator
LLC	LLC resonant converter
OCP	overcurrent protection
OVP	overvoltage protection
PCB	printed circuit board
PF	power factor
PFC	power factor correction
PGND	power ground
PSU	power supply unit
PWM	pulse width modulation
Si	silicon
SiC	silicon carbide
SIPO	series input parallel output
SMPS	switched mode power supply
SR	synchronous rectification
THD	total harmonic distortion
UVLO	undervoltage lockout
UVP	undervoltage protection
VRM	voltage regulator module
WBG	wide bandgap
XFMR	transformer

Revision history

Document revision	Date	Description of changes
V 1.1	2025-05-20	Updated Table 9 – Bill of materials for the control card CD100001427
V 1.0	2025-03-20	Initial release

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2025-05-20

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2025 Infineon Technologies AG. All Rights Reserved.

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

AN101816

Important notice

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Warnings

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.